XTEK CORPOR...
15075C S.W. KOLL PARKWAY
BEAVERTON, OREGON 97006
503-643-1133

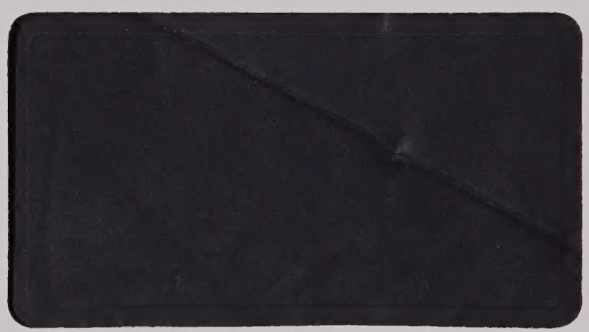
INSTRUCTION MANUAL

MODEL 552A/553A DUAL CHANNEL PROGRAMMABLE FILTER

WAVETEK

WAVETEK SAN DIEGO, INC.

9045 Balboa Ave., San Diego, CA 92123



XTEK CORPORATION
15075C S.W. KOLL PARKWAY
BEAVERTON, OREGON 97006
503-643-1133

INSTRUCTION MANUAL

MODEL 552A/553A DUAL CHANNEL PROGRAMMABLE FILTER

© 1986 Wavetek

THIS DOCUMENT CONTAINS INFORMATION PROPRIETARY TO WAVETEK AND IS SOLELY FOR INSTRUMENT OPERATION AND MAINTENANCE. THE INFORMATION IN THIS DOCUMENT MAY NOT BE DUPLICATED IN ANY MANNER WITHOUT THE PRIOR APPROVAL IN WRITING FROM WAVETEK.

WAVETEK®

WAVETEK SAN DIEGO, INC.
9045 Balboa Ave., San Diego, CA 92123
P. O. Box 85265, San Diego, CA 92138
Tel 619/279-2200 TWX 910/335-2007

Manual Revision: 2/87

WARRANTY

Wavetek warrants that all products manufactured by Wavetek conform to published Wavetek specifications and are free from defects in materials and workmanship for a period of one (1) year from the date of delivery when used under normal operating conditions and within the service conditions for which they were furnished.

The obligation of Wavetek arising from a Warranty claim shall be limited to repairing, or at its option, replacing without charge, any product which in Wavetek's sole opinion proves to be defective within the scope of the Warranty. In the event Wavetek is not able to modify, repair or replace non-conforming defective parts or components to a condition as warrantied within a reasonable time after receipt thereof, Buyers shall be credited for their value at the original purchase price.

Wavetek must be notified in writing of the defect or nonconformity within the Warranty period and the affected product returned to Wavetek's factory or to an authorized service center within (30) days after discovery of such defect or nonconformity.

For product warranties requiring return to Wavetek, products must be returned to a service facility designated by Wavetek. Buyer shall prepay shipping charges, taxes, duties and insurance for products returned to Wavetek for warranty service. Except for products returned to Buyer from another country, Wavetek shall pay for return of products to Buyer.

Wavetek shall have no responsibility hereunder for any defect or damage caused by improper storage, improper installation, unauthorized modification, misuse, neglect, inadequate maintenance, accident or for any product which has been repaired or altered by anyone other than Wavetek or its authorized representative and not in accordance with instructions furnished by Wavetek.

Exclusion of Other Warranties

The Warranty described above is Buyer's sole and exclusive remedy and no other warranty, whether written or oral, is expressed or implied. Wavetek specifically disclaims the implied warranties of merchantability and fitness for a particular purpose. No statement, representation, agreement, or understanding, oral or written, made by an agent, distributor, representative, or employee of Wavetek, which is not contained in the foregoing Warranty will be binding upon Wavetek, unless made in writing and executed by an authorized Wavetek employee. **Under no circumstances shall Wavetek be liable for any direct, indirect, special, incidental, or consequential damages, expenses, losses or delays (including loss of profits) based on contract, tort, or any other legal theory.**

CONTENTS

SECTION 1 GENERAL DESCRIPTION

1.1 INTRODUCTION 1-1
1.2 DEFINITIONS 1-1
1.3 SPECIFICATIONS 1-1
1.3.1 Cutoff Frequency (Fc) 1-1
1.3.2 Full Scale Sensitivity 1-1
1.3.3 Post-Filter Gain 1-1
1.3.4 Low Pass Filter Characteristics 1-1
1.3.5 High Pass Filter Characteristics 1-2
1.3.6 Channel Matching (Model 552A only) 1-2
1.3.7 Input Characteristics 1-2
1.3.8 Output Characteristics 1-2
1.3.9 General 1-2
1.3.10 Options 1-2

SECTION 2 INITIAL PREPARATION

2.1 INSPECTION 2-1
2.2 MECHANICAL INSTALLATION 2-1
2.3 ELECTRICAL INSTALLATION 2-1
2.3.1 Power Connection 2-1
2.3.2 Signal Connection 2-1
2.3.3 GPIB (IEEE-488) Interface 2-1
2.3.4 RS-232-C Interface 2-3
2.4 INITIAL CHECKOUT PROCEDURE 2-4

SECTION 3 OPERATION

3.1 INTRODUCTION 3-1
3.2 CONTROLS AND CONNECTORS 3-1
3.3 TYPICAL OPERATING PROCEDURES 3-1
3.3.1 Mode Selection 3-1
3.3.2 Setting Full Scale Sensitivity 3-2
3.3.3 Setting Cutoff Frequency 3-2
3.3.4 Increment/Decrement Keys 3-2
3.4 REMOTE OPERATION 3-3
3.4.1 General Purpose Interface Bus (GPIB) 3-3
3.4.2 RS-232-C Interface 3-11

SECTION 4 CIRCUIT DESCRIPTION

4.1 INTRODUCTION 4-1
4.2 MAINBOARD 4-1
4.2.1 Attenuator/Amplifier 4-1

CONTENTS (Continued)

4.2.2 Overload Sense 4-3
4.2.3 Filter 4-3
4.2.4 Digital Control Circuitry 4-6
4.2.5 Amplifier/Filter Control 4-8
4.2.6 IEEE-488 Remote Interface 4-8
4.2.7 RS-232-C Remote Interface 4-8
4.2.8 ±12V DC Supply 4-8
4.3 FRONT PANEL BOARD 4-8

SECTION 5 MAINTENANCE

5.1 INTRODUCTION 5-1
5.2 EXTERNAL ATTENUATOR ERROR LOGGING 5-1
5.2.1 Required Test Equipment 5-1
5.2.2 Error Logging Procedure 5-1
5.3 CONFORMANCE TEST PROCEDURE 5-3
5.3.1 Required Test Equipment 5-3
5.4 CALIBRATION 5-16
5.4.1 Factory Calibration 5-16
5.4.2 Required Test Equipment 5-16
5.4.3 Calibration 5-17
5.5 TROUBLESHOOTING 5-31
5.5.1 Factory Repair 5-31
5.5.2 Before You Start 5-31
5.5.3 Isolating a Problem 5-31
5.5.4 Troubleshooting Guides 5-32
5.5.5 Troubleshooting Individual Components 5-44

SECTION 6 PARTS AND SCHEMATICS

6.1 DRAWINGS 6-1
6.2 ADDENDA 6-1
6.3 ORDERING PARTS 6-1

APPENDIXES

A AMERICAN STANDARD CODE FOR INFORMATION INTERCHANGE (ASCII) A-1

ILLUSTRATIONS

Figure 2-1 Voltage Selection and Fuse Replacement 2-1
Figure 2-2 Rear Panel Controls and Connectors 2-2
Figure 2-3 Equipment Setup for Channel 1 and Channel 2 2-4
Figure 3-1 Front Panel Controls and Indicators 3-0
Figure 3-2 LCD Display 3-1
Figure 3-3 GPIB Structure 3-4
Figure 4-1 Model 552A/553A Simplified Block Diagram 4-2
Figure 4-2 Low Pass Filter Block Diagram 4-4
Figure 4-3 Filter Stage Characteristics 4-4

ILLUSTRATIONS (Continued)

Figure 4-4 Second Filter Stage 4-5
Figure 4-5 Digital Control Block Diagram 4-7
Figure 4-6 Front Panel Block Diagram 4-9
Figure 5-1 Desired Results for Calibration Procedure Step 33 5-29
Figure 5-2 Desired Results for Calibration Procedure Step 35 5-29
Figure 5-3 Instrument Connections for Steps 76 Through 78 5-30
Figure 5-4 Mainboard Calibration Points 5-30
Figure 5-5 Amplifier/Filter Control Timing Diagram 5-34
Figure 5-6 DS1 (DS2) Pin Location 5-35

TABLES

Table 2-1 GPIB Data In/Out 2-1
Table 2-2 GPIB Address Codes 2-3
Table 2-3 RS-232-C Connector Pins 2-3
Table 2-4 RS-232-C Configuration Switches 2-3
Table 2-5 Test Equipment and Tools 2-4
Table 2-6 Low Pass Filter Checkout Procedure 2-5
Table 2-7 High Pass Filter Checkout Procedure 2-6
Table 3-1 Class 1 Error Guidelines 3-6
Table 3-2 GPIB Control Parameter Programming Reference Guide 3-8
Table 3-3 GPIB Filter Parameter Programming Reference Guide 3-11
Table 3-4 Class 1 Error Guidelines 3-13
Table 3-5 RS-232-C Interface Control Character Reference Guide 3-15
Table 3-6 RS-232-C Control Parameter Programming Reference Guide 3-16
Table 3-7 RS-232-C Filter Parameter Programming Reference Guide 3-18
Table 5-1 Required Test Equipment 5-1
Table 5-2 Individual Attenuator Switch Errors (Reproducible) 5-2
Table 5-3 Total Attenuation Errors (Reproducible) 5-2
Table 5-4 Required Test Equipment 5-3
Table 5-5 Conformance Procedure 5-5
Table 5-6 Conformance Test Report (Reproducible) 5-11
Table 5-7 Required Test Equipment 5-16
Table 5-8 Calibration Procedure 5-17
Table 5-9 Phase Meter Readings (Reproducible) 5-28
Table 5-10 Fault Isolation 5-31
Table 5-11 Circuit Block Guides 5-32
Table 5-12 Clock Signals 5-33
Table 5-13 U59 Input and Output Line Status 5-33
Table 5-14 U71 (U70) Input and Output Line Status 5-33
Table 5-15 Amplifier/Filter Input Data Lines 5-33
Table 5-16 U7 Output Lines 5-34
Table 5-17 RS-232-C Interface Hardware Checkout 5-36
Table 5-18 IEEE-488 Interface Hardware Checkout 5-37
Table 5-19 Source Voltages Originating From +V0 5-38
Table 5-20 Source Voltages Originating From −V0 5-38
Table 5-21 Relay and FET Status for Selected FULL SCALE Sensitivity 5-38
Table 5-22 Status of Relay Driver U1 (U25) 5-39
Table 5-23 Status of FET Drivers U6/U7 (U30/U31) 5-39
Table 5-24 Analog Signal Voltages in Amplifier/Attenuator Circuit 5-39

TABLES (Continued)

Table 5-25 Source Voltages Originating From +V0 5-40
Table 5-26 Source Voltages Originating From −V0 5-40
Table 5-27 Relays Enabled for Each Cutoff Frequency 5-40
Table 5-28 FETs Enabled for Each Cutoff Frequency 5-40
Table 5-29 Status of Relay Driver U20 (U39) 5-41
Table 5-30 Status of FET Drivers U21/U22 (U43/U44) 5-41
Table 5-31 Analog Signal Voltages in Filter Circuit 5-42
Table 5-32 Source Voltages +V6 (+V12) and −V6 (+V12) 5-42
Table 5-33 Status of K14 (K38) and Relay Driver U20 (U39) 5-42
Table 5-34 Output Amplifier Circuit Voltages 5-43
Table 5-35 Overload Circuit Voltages 5-43
Table 5-36 Power Supply Troubleshooting 5-43
Table 5-37 ±12V DC Supply Voltages 5-43

SAFETY

This instrument is wired for earth grounding via the facility power wiring. Do not bypass earth grounding with two wire extension cords, plug adapters, etc.

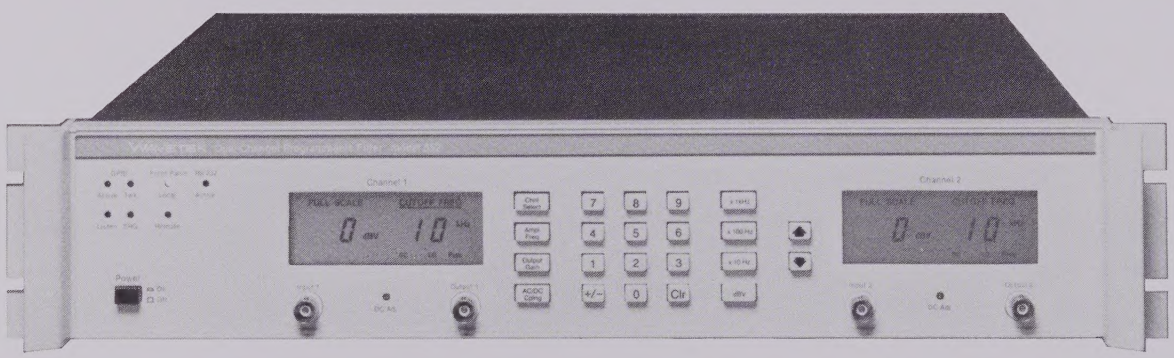
BEFORE PLUGGING IN the instrument, comply with installation instructions.

MAINTENANCE may require power on with the instrument covers removed. This should be done only by qualified personnel aware of the electrical hazards.

The instrument power receptacle is connected to the instrument safety earth terminal with a green/yellow wire. Do not alter this connection. (Reference: ⏚ or ⚠ stamped inside the rear panel near the safety earth terminal.)

WARNING notes call attention to possible injury or death hazards in subsequent operations.

CAUTION notes call attention to possible equipment damage in subsequent operations.



Model 552A, Dual Channel Programmable Filter (Model 553A similar)

SECTION 1
GENERAL DESCRIPTION

1.1 INTRODUCTION

Model 552A is a programmable, two-channel low pass filter. Model 553A differs from the 552A in that it contains one low pass filter and one high pass filter. Both offer exceptional sensitivity and superior performance in the passband and stopband.

The instruments employ 5th-order elliptic filters with 0.5 dB ripple in the passband and greater than 72 dB stopband attenuation. The rolloff transition between passband and stopband is greater than 50 dB per octave.

The cutoff frequency may be programmed from 10 Hz to 50 kHz with 2-digit resolution. Full scale input sensitivity from 1 mVrms (− 60 dBV) to 10 Vrms (+ 20 dBV) is selectable in steps of 5 dB. Another 10 dB of gain may be applied at the filter output.

These instruments are extremely valuable in signal processing applications for band-limiting prior to sampling to prevent aliasing. In addition to the filtering capability, they provide programmable low noise amplification for applications involving low-level signals and overload indicators to ensure operation in their linear range.

The instruments are controlled locally from the front panel using an elastomeric keypad and dual liquid crystal displays showing all filter and gain parameters. The units are controlled remotely via two standard interfaces: IEEE 488 and RS-232-C. Programmed parameters are shown on the front panel displays.

1.2 DEFINITIONS

The cutoff frequency, F_c, is the frequency at which the response of the filter drops below the specified passband ripple, A_{max}. The conventional − 3 dB frequency criterion has no significance in an elliptic filter.

Frequency F_s is the lowest frequency for which the stopband attenuation value, A_{min}, applies.

1.3 SPECIFICATIONS

1.3.1 Cutoff Frequency (F_c)

Range
10 Hz to 50 kHz

Control
Local: Elastomeric digital keypad and dual LCD displays.
Remote (Standard): IEEE 488 and RS-232-C.

Resolution

Multiplier	Frequency (Hz)	Resolution (Hz)
x10	10 — 990	10
x100	1.0 — 9.9K	100
x1K	10K — 50K	1K

Accuracy
− 0% + 3%.

Stability
± 200 ppm/°C.

1.3.2 Full Scale Sensitivity

Range
− 60 dBV (1 mV) to + 20 dBV (10 V) rms full scale.

Resolution
5 dB steps.

Accuracy
± 0.2 dB.

1.3.3 Post-Filter Gain

Range
0 or + 10 dB.

Accuracy
± 0.2 dB.

1.3.4 Low Pass Filter Characteristics

Type
5-pole, 4-zero elliptic.

Rolloff
>53 dB/octave.

Frequency Response

+ 0, − 0.5 dB dc to F_c
− 20 dB at 1.37 F_c (nominal)
− 40 dB at 1.83 F_c (nominal)
− 60 dB at 2.34 F_c (nominal)
− 72 dB above F_s = 2.56 F_c.

1.3.5 High Pass Filter Characteristics (Model 553A Only)

Type
5-pole, 4-zero elliptic.
Rolloff
>53 dB/octave.
Frequency Response
-72 dB below $F_s = 0.39\ F_c$
-60 dB at $0.437\ F_c$ (nominal)
-40 dB at $0.546\ F_c$ (nominal)
-20 dB at $0.730\ F_c$ (nominal)
$+0, -0.5$ dB F_c to 300 kHz
-3 dB at 600 kHz (nominal).

1.3.6 Channel Matching (Model 552A Only)

Amplitude Match (Between Channels with Normalized Gain; See Paragraph 1.3.2).
± 0.1 dB, dc to $0.8\ F_c$, ± 0.2 dB, $>0.8\ F_c$ to F_c.
Phase Match (Between Channels at 0 dBV)
$\pm 1°$ ($\pm 1/2°$ typical) for dc to $0.8\ F_c$.
$\pm 2°$ ($\pm 1°$ typical) for $>0.8F_c$ to F_c.

1.3.7 Input Characteristics

Coupling
DC (low pass filter only) or ac with nominal 0.5 Hz cutoff.
AC coupling forced for full scale sensitivity from -40 dBV to -60 dBV.
Impedance
1 MΩ and 50 pF nominal.
Equivalent Input Noise
-150 dBV/Hz (-160 dBV/Hz typical) at 1 kHz with -60 dBV full scale sensitivity setting.

1.3.8 Output Characteristics

Impedance
50 Ω nominal.
Full Scale Signal
1 Vrms into $R_L > 5$ kΩ, no output gain.
3.16 Vrms into $R_L > 5$ kΩ, $+10$ dB output gain.
Noise (1 MHz detector BW)
>80 dB below full scale referred to output at $+20$ dBV full scale sensitivity.
<10 μV referred to input at -60dB full scale sensitivity.
Harmonic Components
>72 dB below full scale for 1 kHz input signal.
Spurious Components
>72 dB below full scale (includes line-related spurious) for full scale sensivity from $+20$ dBV to -50 dBV.
>65 dB below full scale, for full scale sensitivity at -55 dBV
>60 dB below full scale, for full scale sensitivity at -60 dBV.
Intermodulation Products
>70 dB below full scale for 40 kHz and 50 kHz input frequencies.
DC Offset
$<\pm 10$ mV, adjustable to 0 Vdc.
DC Drift
± 50 mV maximum, $+15°$ to $+40°$C at 0 dB full scale sensitivity setting.

1.3.9 General

Configuration
Bench top, convertable to rack mounting.
Input/Output Connectors
Front panel BNCs.
Accessories Supplied
Instruction manual, line cord.
Temperature
0°C to $+40$°C for operation; -20°C to $+70$°C for storage.
Dimensions
43.2 cm (17 in) wide; 8.9 cm (3.5 in) high; 41.3 cm (16.3 in) deep.
Weight
33 kg (15 lb) net.
Power
100/120/220/240 Vac $\pm 10\%$, 50 to 60 Hz, 50 VA.

1.3.10 Options

004: Rack Mounting Kit

SECTION 2
INITIAL PREPARATION

2.1 INSPECTION

After unpacking the instrument, visually inspect all external parts for possible damage to connectors, surface areas, etc. If damage is discovered, file a claim with the carrier who transported the unit. The shipping container and packing materials should be saved in case reshipment is required.

2.2 MECHANICAL INSTALLATION

The instrument can be used on bench top or standard 19-inch RETMA rack mounted. Ambient temperature within the rack must not exceed + 40°C while the instrument is operating. The rear panel switches should be set before installing the filter in the rack.

2.3 ELECTRICAL INSTALLATION

2.3.1 Power Connection

The instrument will operate from any of the following line voltages: 100, 120, 220 or 240 Vac ± 10%, 50 to 60 Hz. Voltage selection is made using the card inside the power cord receptacle on the rear panel. (See figure 2-1.)

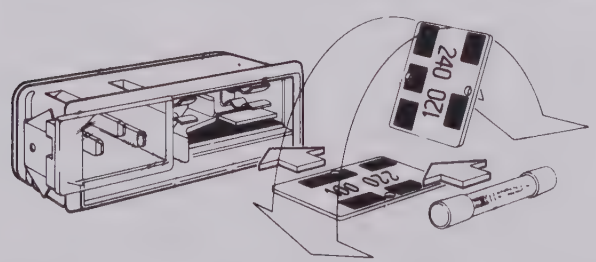


Figure 2-1. Voltage Selection and Fuse Replacement

WARNING

In keeping with standard safety practice, the case of the instrument is grounded through the 3-pronged power cord. If the instrument must be connected to a two slot receptacle, use a parallel ground adapter and connect the remaining lead to ground.

The line fuse is also contained inside the instruments power cord receptacle. For 100 or 120 Vac operation, the fuse should be a 1/2A SB fuse; for 220 or 240 Vac operation it should be a 1/4A SB fuse.

2.3.2 Signal Connection

Use RG58U 50 Ω coaxial cables when connecting this instrument to associated equipment.

2.3.3 GPIB (IEEE-488) Interface

2.3.3.1 GPIB Connection

The GPIB (IEEE-488) I/O rear panel connection is shown in figure 2-2; pin connections and signal names are given in table 2-1.

Table 2-1. GPIB Data In/Out

Pin	Signal	
1	DIO1	True When Low
2	DIO2	
3	DIO3	
4	DIO4	
5	EOI	
6	DAV	
7	NRFD	True When High
8	NDAC	
9	IFC	True When Low
10	SRQ	
11	ATN	
12	Chassis Ground (⏚)	
13	DIO5	True When Low
14	DIO6	
15	DIO7	
16	DIO8	
17	REN	
18	GND	Signal Gnd (⏚)
19	GND	
20	GND	
21	GND	
22	GND	
23	GND	
24	GND	

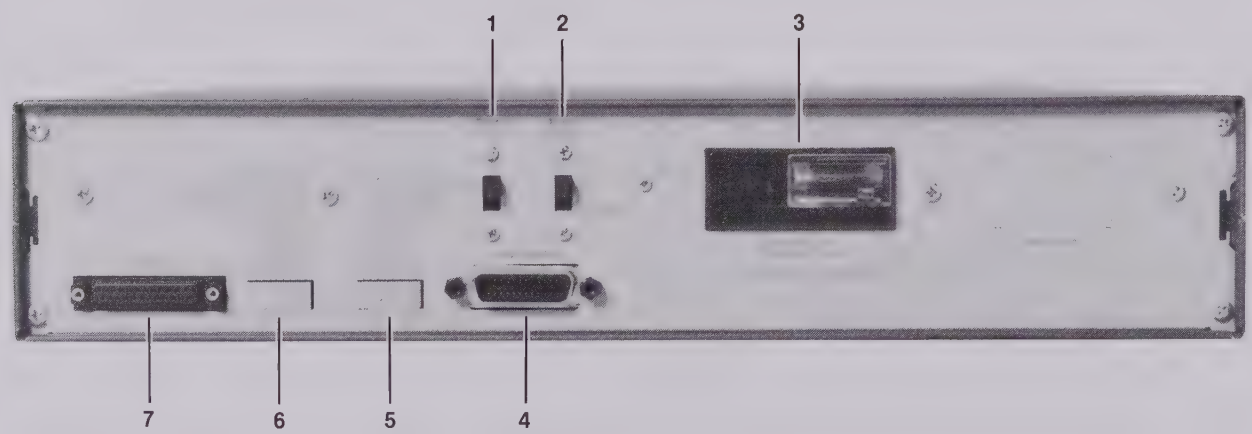
The GPIB panel connector is equivalent to an Amphenol 57-10240 and connectes to a standard GPIB bus cable connector (available from Wavetek in 1 and 2 meter lengths).

2.3.3.2 GPIB Address

Each instrument on the General Purpose Interface Bus (GPIB), must have its GPIB bus address appropriately set. The GPIB address may be selected by the rear panel switch, item 5, shown in figure 2-2 and table 2-2. The five address switch sections are labeled on the panel with the binary weight of each switch. The bit weight is ON (= 1) in the up position of the switch and OFF (= 0) in the down position.

The LISTEN ALWAYS switch activates this mode in the up position and causes normal addressed operation in the down position.

The SHIELD switch connects the bus cable shield pin to signal ground in the up postion.



Loc	Function
1	Digital Common Float/Ground Switch
2	Analog Common Float/Ground Switch
3	AC Power Receptacle — For IEC power cord; includes fuseholder and line voltage selector
4	GPIB (IEEE 488) Connector
5	GPIB (IEEE 488) Configuration Switch
6	RS-232-C Configuration Switch
7	RS-232-C Connector — Female DB-25S style

Figure 2-2. Rear Panel Controls and Connectors

Table 2-2. GPIB Address Codes

Device	ASCII		Switch Position	Hexa-decimal	
	Listen	Talk	Weight	Listen	Talk
0	(space)	@	0 0 0 0 0	20	40
1	!	A	1 0 0 0 0	21	41
2	"	B	0 1 0 0 0	22	42
3	#	C	1 1 0 0 0	23	43
4	$	D	0 0 1 0 0	24	44
5	%	E	1 0 1 0 0	25	45
6	&	F	0 1 1 0 0	26	46
7	'	G	1 1 0 0 0	27	47
8	(	H	0 0 0 1 0	28	48
9	)	I	1 0 0 1 0	29	49
10	*	J	0 1 0 1 0	2A	4A
11	+	K	1 1 0 1 0	2B	4B
12	,	L	0 0 1 1 0	2C	4C
13	—	M	1 0 1 1 0	2D	4D
14	.	N	0 1 1 1 0	2E	4E
15	/	O	1 1 1 1 0	2F	4F
16	0	P	0 0 0 0 1	30	50
17	1	Q	1 0 0 0 1	31	51
18	2	R	0 1 0 0 1	32	52
19	3	S	1 1 0 0 1	33	53
20	4	T	0 0 1 0 1	34	54
21	5	U	1 0 1 0 1	35	55
22	6	V	0 1 1 0 1	36	56
23	7	W	1 1 1 0 1	37	57
24	8	X	0 0 0 1 1	38	58
25	9	Y	1 0 0 1 1	39	59
26	:	Z	0 1 0 1 1	3A	5A
27	;	[	1 1 0 1 1	3B	5B
28	<	\	0 0 1 1 1	3C	5C
29	=	]	1 0 1 1 1	3D	5D
30	>	↑	0 1 1 1 1	3E	5E

NOTE
Address 31 is not allowed.

2.3.4 RS-232-C Interface

2.3.4.1 RS-232-C Connection

A standard DB-25F (female) connector on the rear panel of the instrument provides connections for RS-232-C signals. The mating connector should be equivalent to a DB-25P (male) connector, commonly available from computer or electronic accessory suppliers.

The wiring of the connector conforms to that for DCE (Data Communication Equipment). The signals present are listed in Table 2-3

Table 2-3. RS-232-C Connector Pins

Pin	Signal	In/Out	Description
1	PG	—	Protective Ground
2	RxD	IN	Receive Data
3	TxD	OUT	Transmitted Data
4	RTS	IN	Request to Send
5	CTS	OUT	Clear to Send
6	DSR	OUT	Data Set Ready
7	GND	—	Signal Ground
8	CD	IN	Carrier Detect*
20	DTR	IN	Data Terminal Ready

Pin numbers not shown in the above chart have no internal connection.

*Line CD is connected to a line receiver but has no interface function.

2.3.4.2 RS-232-C Configuration

The RS-232-C configuration switches on the rear panel shown in figure 2-2, are used to set parity, stop bit and baud rate for the RS-232-C port. Table 2-4 shows the function of each switch.

Table 2-4. RS-232-C Configuration Switches

Switch	Function	Position	Effect
1	Shield	UP	Protective GND tied to Signal GND
		DN	Protective GND floating
2	Stop Bits	UP	2 Stop Bits
		DN	1 Stop Bit
3	Data Bits	UP	8 Data Bits
		DN	7 Data Bits
4	Parity	UP	Odd Parity
		DN	Even Parity
5	Parity Inh	UP	Parity Inhibited
		DN	Parity Enabled
6,7,8	Baud Rate	UP	= Logic 1
		DN	= Logic 0

Switch 6 7 8	Baud Rate
0 0 0	110
0 0 1	150
0 1 0	300
0 1 1	600
1 0 0	1200
1 0 1	2400
1 1 0	4800
1 1 1	9600

2.3.4.3 Connecting the RS-232-C Interface

To connect the instrument to a RS-232-C device, the manual for the other device should be examined to determine the pinout of its RS-232-C connector. Most devices using the RS-232-C interface will have a DB-25 type connector and standard interconnection cabling can be used. In some cases, due to special connectors or pin assignments, a special cable will have to be made.

The method of handshaking which is fully described in section 3 will determine which lines are required. The two types of handshaking are XON/XOFF (software) and CTS/RTS (hardware). With XON/XOFF handshaking and software control of the RS-232-C mode, the minimal interface can consist of three lines: TxD, RxD, and GND.

2.4 INITIAL CHECKOUT PROCEDURE

The checkout procedure in tables 2-6 and 2-7 are to be used only as receiving inspection or post-repair checkout. They are not intended to verify all specifications.

A list of test equipment is given in table 2-5. Follow each step given in order and verify the results.

Table 2-5 Test Equipment and Tools

Oscilloscope:	Bandwidth > 100 MHz
Freq Synthesizer:	90 Hz to 20 kHz
Attenuator:	0 to 20 dB, 5dB steps
BNC Coax Cables:	RG58U, 3 ft., 3 ea
BNC Tee:	1 male, 2 female

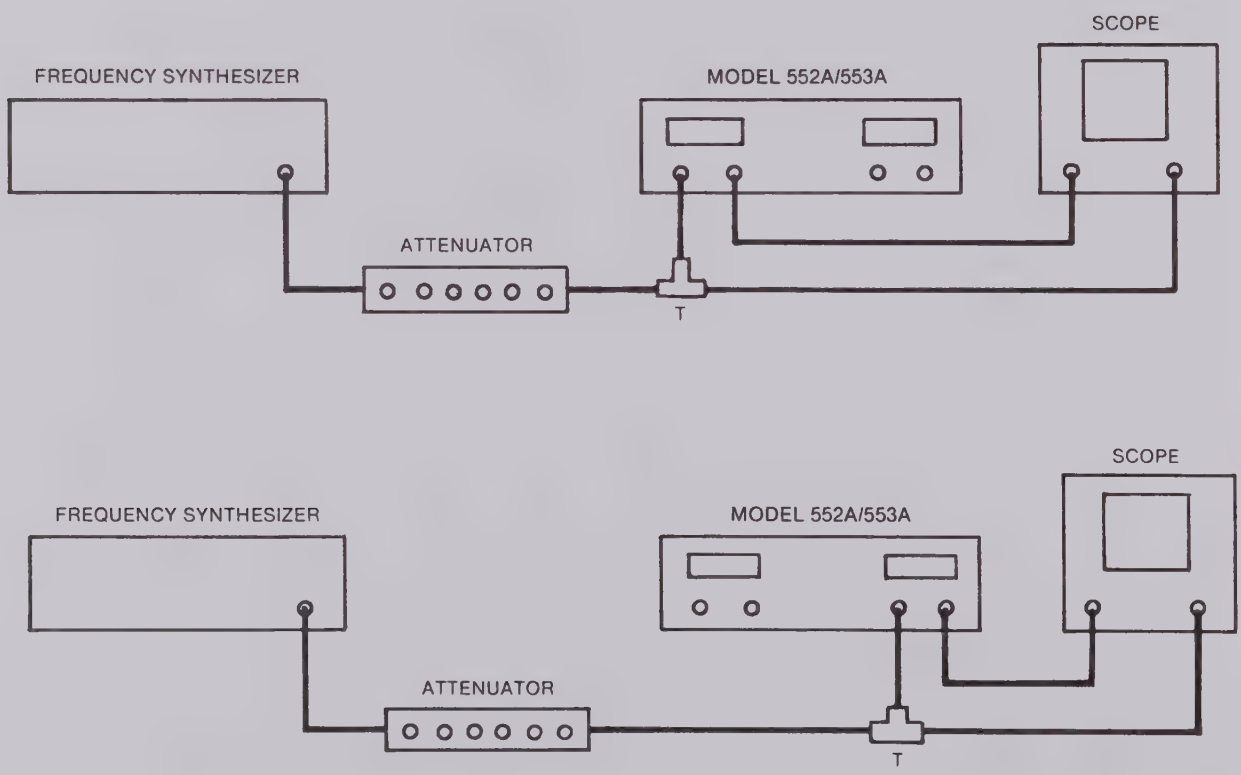


Figure 2-3. Equipment Setup for Channel 1 (Top) and Channel 2 (Bottom)

Table 2-6. Low Pass Filter Checkout Procedure

Step	Control	Operation	Observation
1	**Power**	**On**	All LED's flash, then **Local** LED stays on. LCD's indicate 0 dBV, DC and 10 kHz, on both channels. Cursor (underline) under CUTOFF FREQ, on **Channel 1** only
2	**Channel Select**	Press once	Cursor under CUTOFF FREQ on **Channel 2**
3	**Channel Select**	Press once	Cursor under CUTOFF FREQ on both channels
4	**1**	Press once	Both cursors flash, 1 kHz displayed on both channels
5	**0**	Press once	10 kHz displayed on both channels
6	**X10 Hz**	Press once	Cursors stop flashing, .10 kHz displayed on both channels
7	*(Set Synthesizer to 90 Hz)*		2 V p-p on scope Ch 1. Verify 2 V p-p on scope Ch 2
8	*(Set Synthesizer to 200 Hz)*		Verify about 10 mV p-p on scope Ch 2
9	**X100 Hz**	Press once	1.0 kHz displayed on both channels
10	*(Set Synthesizer to 900 Hz)*		Verify 2 V p-p on scope Ch 2
11	*(Set Synthesizer to 2 kHz)*		Verify about 10 mV p-p on scope Ch 2
12	**X1kHz**	Press once	10 kHz displayed on both channels
13	*(Set Synthesizer to 9 kHz)*		Verify 2 V p-p on scope Ch 2
14	*(Set Synthesizer to 20 kHz)*		Verify about 10 mV p-p on scope Ch 2
15	**Ampl Freq**	Press once	Cursors under FULL SCALE on both channels
16	*(Set Synthesizer to 1 kHz*		Verify 2 V p-p on scope Ch 2
17	⬇	Press once	FULL SCALE reading shows – 5 dBV on both channels
18	*(Set Attenuator to 5 dB)*		Verify 2 V p-p on scope Ch 2
19	**2**	Press once	– 2 dBV on both displays, both cursors flashing
20	**0**	Press once	– 20 dBV on both displays
21	**dBV**	Press once	– 20 dBV on both displays, cursors stop flashing

Table 2-6. Low Pass Filter Checkout Procedure (Continued)

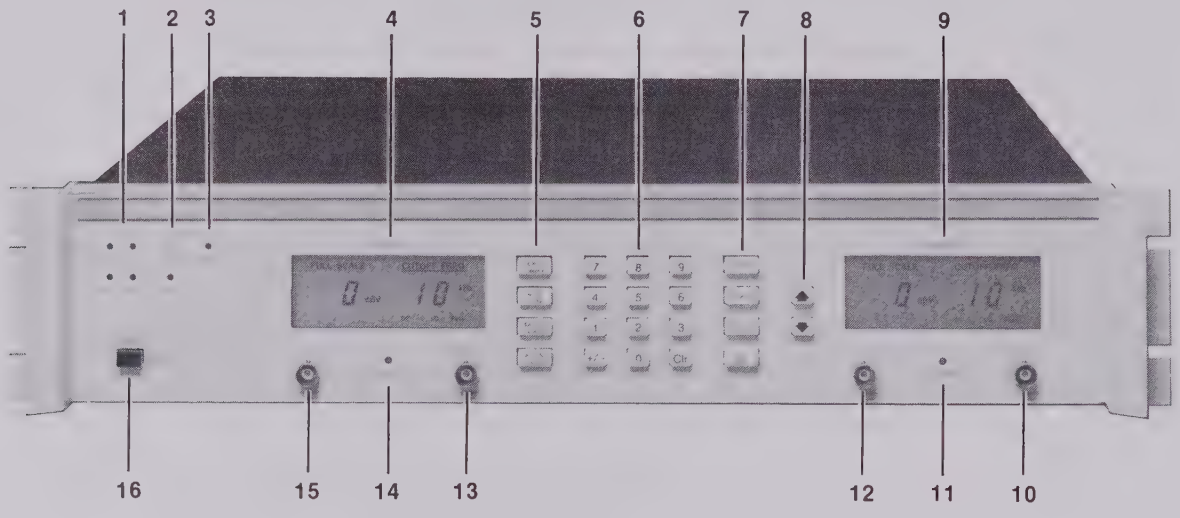
Step	Control	Operation	Observation
22	*(Set Attenuator to 20 dB)*		Verify 2 V p-p on scope Ch 2
23	**+/–**	Press once	+ 20 dBV on both displays, cursors flashing
24	**dBV**	Press once	+ 20 dBV on both displays, cursors stop flashing
25	*(Set Attenuator to 0 dB)*		Verify about 0.2 V p-p on scope Ch 2
26	**Output Gain**	Press once	Verify + 10 dB Output Gain message on display on both channels. Verify about 0.63 V p-p on scope Ch 2

Table 2-7. High Pass Filter Checkout Procedure (Model 553A Only)

Step	Control	Operation	Observation
1	**Power**	**On**	All LED's flash, then **Local** LED stays on. LCD's indicate 0 dBV, DC and 10 kHz, on both channels. Cursor (underline) under CUTOFF FREQ, on **Channel 1** only
2	**Channel Select**	Press once	Cursor under CUTOFF FREQ on **Channel 2**
3	**Channel Select**	Press once	Cursor under CUTOFF FREQ on both channels
4	**1**	Press once	Both cursors flash, 1 kHz displayed on both channels
5	**0**	Press once	10 kHz displayed on both channels
6	**X10 Hz**	Press once	Cursors stop flashing, .10 kHz displayed on both channels
7	*(Set Synthesizer to 110 Hz)*		2 V p-p on scope Ch 1. Verify 2 V p-p on scope Ch 2
8	*(Set Synthesizer to 50 Hz)*		Verify about 10 mV p-p on scope Ch 2
9	**X100 Hz**	Press once	1.0 kHz displayed on both channels
10	*(Set Synthesizer to 1100 Hz)*		Verify 2 V p-p on scope Ch 2
11	*(Set Synthesizer to 500 Hz)*		Verify about 10 mV p-p on scope Ch 2
12	**X1kHz**	Press once	10 kHz displayed on both channels

Table 2-7. High Pass Filter Checkout Procedure (Continued)

Step	Control	Operation	Observation
13	*(Set Synthesizer to 11 kHz)*		Verify 2 V p-p on scope Ch 2
14	*(Set Synthesizer to 5 kHz)*		Verify about 10 mV p-p on scope Ch 2
15	**X10 Hz**	Press once	Cursors stop flashing, .10 kHz displayed on both channels
16	**Ampl Freq**	Press once	Cursors under FULL SCALE on both channels
17	*(Set Synthesizer to 1 kHz*		Verify 2 V p-p on scope Ch 2
18	⬇	Press once	FULL SCALE reading shows −5 dBV on both channels
19	*(Set Attenuator to 5 dB)*		Verify 2 V p-p on scope Ch 2
20	**2**	Press once	−2 dBV on both displays, both cursors flashing
21	**0**	Press once	−20 dBV on both displays
22	**dBV**	Press once	−20 dBV on both displays, cursors stop flashing
23	*(Set Attenuator to 20 dB)*		Verify 2 V p-p on scope Ch 2
24	**+/−**	Press once	+ 20 dBV on both displays, cursors flashing
25	**dBV**	Press once	+ 20 dBV on both displays, cursors stop flashing
26	*(Set Attenuator to 0 dB)*		Verify about 0.2 V p-p on scope Ch 2
27	**Output Gain**	Press once	Verify + 10 dB Output Gain message on display on both channels. Verify about 0.63 V p-p on scope Ch 2



Controls and Indicators

Loc	Function
1	**GPIB** Status Indicators — Displays the status of the GPIB interface.
2	**Front Panel** Status Indicators — Front panel keyboard is active in **Local** and disabled in **Remote**.
3	**RS 232** Status Indicator — Displays status of RS-232-C remote interface.
4	**Channel 1** LCD Display — Displays cutoff frequency, sensitivity, input coupling and output gain for channel 1.
5	Mode Select Keypad — Selects parameter to be loaded via the front panel.
6	Numeric Keypad — Used for front panel entry of cutoff frequency and sensitivity data.
7	Units Keypad — Used for entering the frequency multiplier or dBV terminator for keypad data entries.

Loc	Function
8	Increment, Decrement Keypad — Used for incrementing or decrementing either cutoff frequency or sensitivity.
9	**Channel 2** LCD Display — Displays cutoff frequency, sensitivity, input coupling and output gain for channel 2.
10	**Output 2** — Channel 2 output BNC.
11	**DC Adjust** — DC Level adjustment for channel 2.
12	**Input 2** — Channel 2 input BNC.
13	**Output 1**— Channel 1 output BNC.
14	**DC Adjust (Model 552A only)** — DC level adjustment for channel 1.
15	**Input 1** Channel 1 input BNC.
16	**Power** Switch — Controls ac line power to instrument.

Figure 3-1. Front Panel Controls and Indicators

SECTION 3
OPERATION

3.1 INTRODUCTION

This section describes how to operate the instrument. The controls and front panel indicators are shown, followed by typical operating procedures and response characteristics. Finally, the GPIB and RS-232-C interfaces are explained.

3.2 CONTROLS AND INDICATORS

The front panel controls and displays are shown in figure 3-1. The rear panel features appear in figure 2-2. The LCD display is described in figure 3-2.

3.3 Typical Operating Procedures

The dual LCD's (liquid crystal displays) on the front panel reflect the current operating status of the filters, whether controlled from the front panel (local) or through one of the remote interfaces.

There are two general rules regarding the operation of the front panel keypad and LCD displays:

- The cursors (solid lines underneath the FULL SCALE and CUTOFF FREQ legends) when displayed, show where keyboard data will be directed. If the cursor is flashing, data entry is in process and the display reflects a partial or unterminated value.
- The value displayed after data entry (cursor not flashing) is always the actual operating value of the filter. If an illegal or out of range value was entered, the nearest valid value is chosen.

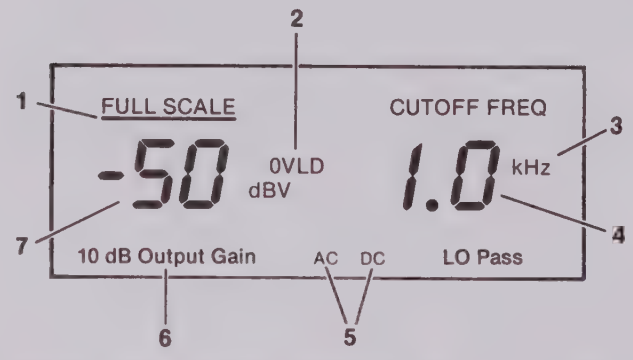
3.3.1 Mode Selection

Channel Selection

The **Channel Select** key causes the cursor to shift among three modes: **Channel 1** only, **Channel 2** only, or both channels. Each time this key is pressed, the cursor will shift and display either one or both LCD's.

Amplitude/Frequency Select

The **Ampl/Freq** key toggles the cursor position within the selected channel(s) to either FULL SCALE sensitivity (amplitude) or CUTOFF FREQuency. Each time this key is pressed, the cursor shifts to the alternate position.



Loc	Function
1	Cursor — Solid line under the FULL SCALE legend indicates Full Scale program mode. Solid line under the CUTOFF FREQ legend indicates the Cutoff Frequency program mode.
2	OVLD Indicator — Indicates an overload condition when flashing.
3	Cutoff Frequency Multiplier — Shows either Hz or kHz multiplier for cutoff frequency digits.
4	Cutoff Frequency Digits — Two digits with decimal point showing the cutoff frequency setting.
5	Input Coupling Mode — Displays either AC or DC (low pass filter only) input coupling status.
6	Output Gain Status — Displays either nothing (0 dB) or 10 dB Output Gain status.
7	Full Scale Sensitivity Digits — Two digits plus polarity showing the full scale sensitivity setting.

Figure 3-2. LCD Display

Output Gain Selection

The **Output Gain** key toggles the output gain state in the channel(s) where the cursor is displayed (for either FULL SCALE or CUTOFF FREQuency.) Each time the key is pressed, the output gain for the selected channel(s) will toggle between the two values 0 dB and 10 dB; shown in the LCD's as nothing (0 dB) or "10 dB Output Gain".

Input Coupling Selection (Low Pass Filter Only)

The **AC/DC Coupling** key toggles the input coupling function in the channel(s) where the cursor is displayed (for either FULL SCALE or CUTOFF FREQuency). Each time the key is pressed, the input coupling for the selected channel(s) will toggle between AC and DC coupling, as shown in the LCD's.

NOTE

For full scale sensitivity values between −60 dBV and −40 dBV, the input is forced to be AC coupled.

3.3.2 Setting Full Scale Sensitivity

The full scale sensitivity setting sets the input gain section of the filter to accomodate the amplitude of the signal at the input BNC. To maximize the useful dynamic range, the full scale sensitivity should be set as low as possible. Unit sensitivity increases (more gain is provided) as the full scale setting decreases. If the full scale sensitivity is set too low, the signal will cause an overload condition and may lead to distortion of the signal. This condition is indicated by the OVLD message on the LCD corresponding to the overloaded channel. If this occurs, the full scale sensitivity value should be increased until the OVLD message disappears.

Full scale sensitivity can be selected between the values of −60 dBV (1 mV) rms and +20 dBV (10 V) rms, in steps of 5 dB. All invalid data entries are adjusted toward less sensitivity.

NOTE

For full scale sensitivity values between −60 dBV and −40 dBV, the input is forced to be AC coupled.

To enter data, first use the **Channel Select** key and the **Ampl/Freq** key to activite the cursor for the desired channel(s). The numeric keys (**0** through **9**) are used to enter the two digit value for full scale input sensitvity. The **+/−** key will toggle the polarity of the data entry each time it is pressed. The **Clr** key will discard any data entry and restore the current operating value to the display.

The **dBV** key terminates the FULL SCALE sensitivity data entry and transfers it to the control section of the selected channel(s).

3.3.3 Setting Cutoff Frequency

The cutoff frequency defines the upper limit of the passband for the low pass filter and the passband lower limit for the high pass filter. It may be set from 10 Hz to 90 Hz with one-digit resolution and from 100 Hz to 50 kHz with two-digit resolution.

To enter data, first use the **Channel Select** key and the **Ampl/Freq** key to activite the cursor for the desired channel(s). The numeric keys (**0** through **9**) are used to enter a one- or two-digit value for CUTOFF FREQuency. The **+/−** key has no effect. The **Clr** key causes any data entered to be discarded, and the display is restored to the current active value.

One of the three frequency multiplier keys, **x10Hz**, **x100Hz**, or **x1kHz**, is then pressed to terminate the entry. The new CUTOFF FREQuency is then loaded to the control section of the selected channel(s).

Some values of CUTOFF FREQuency may be entered two different ways, using two different multiplier keys. The filter performance will be the same in either case. For example, a CUTOFF FREQuency of 1 kHz can be entered either as **1**,**0, x100Hz** or as **1**, **x1kHz**. In both cases, the LCD will show 1.0 kHz and the filter will operate identically.

There is some overlap between multiplier ranges. For example, using the **x1kHz** multiplier, the user can enter consecutive frequencies of 1 x1kHz, 2 x1kHz, etc., providing resolution of 1 kHz between frequencies. Alternately, using the **x100 Hz** multiplier, the user can enter consecutive frequencies of 10 x100Hz, 11 x100Hz, etc., covering the same frequency range as above but now with 100 Hz resolution between frequencies instead of 1 kHz. The extra resolution can be important in many applications.

3.3.4 Increment/Decrement Keys

The two keys labled with the up arrow and down arrow provide an easy means of adjusting or stepping the operating values for FULL SCALE sensitivity or CUTOFF FREQuency. The cursor determines which parameters are affected by the arrow keys. If the cursors are active in both channels, then both channels will be affected.

In the case where FULL SCALE sensitivity is selected, the value will be incremented or decremented by 5 dB each time one of the arrow keys is pressed.

When CUTOFF FREQuency is selected, each pressing of the arrow keys will increment or decrement the cutoff frequency value by the smallest frequency resolution step available.

If an arrow key is held in the pressed position, after an initial delay, the selected value will keep stepping several times per second until the key is released. Only after the key is released will the final value shown on the LCD be loaded to the control section of the filter.

The arrow keys have no effect on input coupling or output gain.

3.4 REMOTE OPERATION

Introduction

The standard instrument includes both GPIB (General Purpose Interface Bus) and RS-232-C remote interfaces. Language programmed for both is essentially the same. In addition, there is exchange of some program commands such as RS-232-C UART status being readable over the GPIB interface. Even with these similarities, each interface has its own hardware configuration and interface control commands.

Remote Interface Priority

If the RS-232-C and GPIB remote interfaces are used alternately, the instrument will respond correctly. However, only one interface can be active at any given moment. If there is conflict between the two interfaces, RS-232-C takes priority over GPIB. Programmed values and instrument status do not change when exiting and entering the remote modes. As explained in paragraph 3.4.2.3, either a low-to-high transition on the RS-232-C DTR line or the receipt of a '!' on the RS-232-C port while the GPIB mode is active will abort the GPIB mode and reset the active LISTEN or TALK state. Any GPIB command sequence in progress will be lost and control must be re-established after the RS-232-C mode is exited before any programming from the GPIB interface is possible.

CAUTION

If the state of the DTR line is changed or a '!' is sent to the RS-232-C port during any GPIB or RS-232-C data transfer, unpredictable results may occur.

Both interfaces have priority over front panel control, which can be enabled or disabled by the active interface. Unless disabled by command, the front panel remains enabled by default. The two front panel disable commands from the GPIB interface are 'LL0' and 'L0'. If 'LLO' is used, front panel control can only be reinstated by sending 'GTL' (Go To Local) over the GPIB bus. If the GPIB disables the front panel with the 'L0' command, the 'L1' command will restore front panel control. The only front panel disable command from the RS-232-C interface is 'L0'. Front panel control is regained by sending 'L1' over the RS-232-C interface.

3.4.1 The General Purpose Interface Bus (GPIB)

The GPIB interface is an implementation of IEEE specification 488-1978. It supports the following interface functions which are described in detail in the specification. Relevant aspects of these functions are discussed in following paragraphs.

SH1	Complete source handshake.
AH1	Complete acceptor handshake.
T6	Basic talker.
TE0	No extended talker.
L3	Basic listener.
LE0	No extended talker.
SR1	Complete service request.
RL1	Remote/local and local lockout.
PP1	Parallel poll.
DC1	Device clear and selective device clear.
DT1	Complete device trigger.
C0	No controller.
E2	Tri-state drivers.

Instruments on the bus may have "talk" and "listen" capabilities. The talk capability allows a device to send data (such as error message readings) out over the bus. The listen capability allows a device to receive data (such as device programming information) from the bus.

The GPIB consists of 16 negative true signal lines as shown in figure 3-3. These 16 lines include 8 bidirectional data lines, 3 handshake lines and 5 control lines. All devices on the bus interface to these lines with passive pull up and active pull down. Thus, any device may "assert" a line by pulling it down to the logic low, or "true" state. If no device is asserting the line, it is pulled up to the logic high, or "false" state. (Only the controller is allowed to assert certain lines.)

As shown in figure 3-3, devices connected to the bus may be a LISTENER (only), TALKER (only), LISTENER/TALKER or CONTROLLER. More than one controller may be connected to the bus, but only one controller may be hard wired as SYSTEM CONTROLLER, and only one controller at a time may assume the role of ACTIVE CONTROLLER.

3.4.1.1 Bus Line Definitions

The 16 negative-true GPIB signal lines are:

DIO1-DIO8	Data In/Out Lines
ATN	Attention
REN	Remote Enable
DAV	Data Available
NRFD	Not Ready For Data
NDAC	Not Data Accepted

EOI	End Or Identify
SRQ	Service Request
IFC	Interface Clear

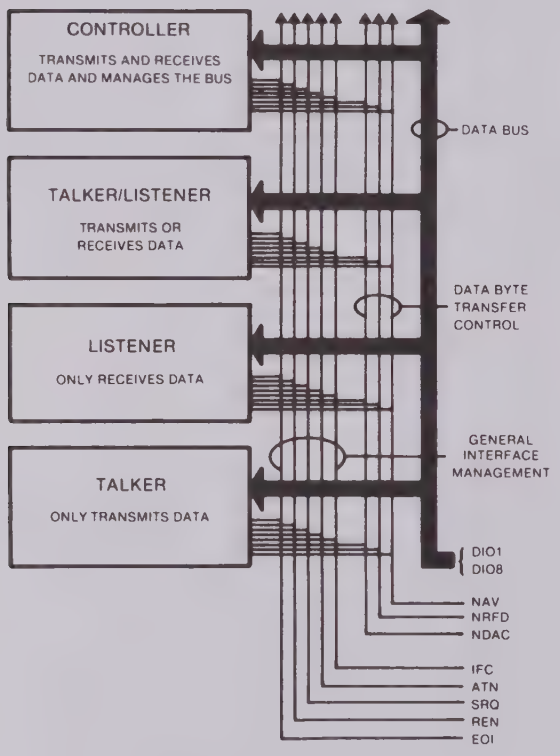


Figure 3-3. GPIB Structure

The functions of the GPIB signal lines are:

DIO1-DIO8 — These eight lines (Data In/Out) are used to send commands from the controller and to transfer data back and forth between instruments and the controller.

ATN — The Attention line is operated only by the active controller. It specifies whether the information on lines DIO1-DIO8 is data (ATN false) or a command (ATN true). Whenever ATN is set true, no activity is allowed on the bus except for controller originated messages.

REN — The Remote Enable line controls whether devices on the GPIB are in local or remote modes. The instrument enters the remote state when it receives its listen address and REN is enabled. It then remains in the remote mode until the REN line is put in the local state, a Go To Local (GTL) command is received or the RS-232-C bus takes control.

DAV, NRFD, NDAC — These are the "handshake" lines (Data Valid, Not Ready For Data and Not Data Accepted) which regulate the transmission of information over the lines DIO1-DIO8. For each command or data byte transferred, a complete handshake cycle occurs. This handshake is designed to hold up the bus until the slowest device has accepted the information.

EOI — When ATN is false, EOI (End Or Identify) indicates that the data on lines DIO1-DIO8 is the last byte of a data message. When the instrument receives a data byte with EOI true, it automatically supplies a terminator character following the data byte. When it transmits the last byte of a message (which is always a terminator character) it also sets EOI true.

SRQ — The Service Request line is used by the instrument and other devices on the bus to signal the controller that they request attention. Since the SRQ line is common to all devices, additional tests must be made to determine which devices are signaling. The controller performs either a Serial or Parallel Poll to accomplish this.

IFC — The Interface Clear line is asserted by the system controller to reset the interface logic in all devices connected to the bus to a known initial state.

3.4.1.2 Handshake Sequence

The three handshake lines, Data Valid (DAV), Not Ready for Data (NRFD) and Not Data Accepted (NDAC) are used in a typical data exchange as described in the next paragraph.

All devices currently designated as active listeners would indicate (via the NRFD line) when they are ready for data. A device not ready would pull this line low (ground), while a device that is ready would let the line float high. Since

a low overrides a passive high, this line will stay low until all active listeners are ready for data. When the talker senses this, it places the next data byte on the data lines and then pulls DAV low. This tells the listeners that the information on the data lines is valid and that they may read it. Each listener (at its own speed) then takes the data and lets the NDAC line go high. Again, only when all listeners have let NDAC go high will the talker sense that all listeners have read the data. It can then remove DAV (let it go high) and start the entire sequence over again for the next byte of data.

3.4.1.3 Commands

Commands are sent over lines DIO1-DIO8 with ATN true. They are divided into five classes:

1. Listen Addresses
2. Talk Addresses
3. Secondary Addresses
4. Universal Commands
   DCL Device Clear
   SPE Serial Poll Enable
   SPD Serial Poll Disable
   LLO Local Lockout
5. Addressed Commands
   GTL Go To Local
   SDC Selective Device Clear
   GET Group Execute Trigger

Listen Address

Listen addresses are used to command a device to read any data bytes transmitted over lines DIO1-DIO8. There are 31 different available addresses (hexadecimal codes 20 through 3E shown in table 2-2). The unlisten address (hexadecimal 3F) is used to command all devices to not read data bytes. The instrument listen address is selected by rear panel switches as shown in figure 2-2. If the instrument is to be a listener only, see paragraph 3.4.1.4.

Talk Address

Talk addresses are used to command a device to transmit data over lines DIO1-DIO8. There are 31 different available addresses shown in table 2-2 (hexadecimal codes 40 through 5E, ASCII codes @ through ↑). A 32nd address, called untalk (hexadecimal 5F, ASCII "_") is used to command all devices to cease talking. The lower 5 bits of the instrument talk address are selected by the same switches used to select the listen address. Thus, if the instrument listen address is hexadecimal 21 (ASCII "!"), the talk address is hexadecimal 41 (ASCII "A").

Secondary Address

Secondary addresses are used following a talk or listen address to provide the ability to address more than the 31 devices provided for by simple talk or listen addresses. Secondary addresses are ignored by the instrument.

Universal Commands

Universal commands are used to command a device to perform designated actions. Universal commands are recognized at all times. Universal commands performed by the instrument are:

1. Device Clear (DCL) — Resets the instrument to the power on default settings. DCL affects all devices on the bus.
2. Serial Poll Enable (SPE) — Causes the instrument to engage in a serial poll by responding with the serial poll status byte when addressed as a talker. Data line DIO7 will be on, if service is being requested on the SRQ line. When the status byte is read, it is reset to all zeros, and the SRQ line is released (of course, it may still be held down by other devices). The status byte is also available by reading the instrument talk mode T1 message. When this message is read, the status byte is reset and the SRQ released as for the serial poll.
3. Serial Poll Disable (SPD) — Discontinues serial poll. Returns instrument to normal talk modes.
4. Local Lockout (LLO) — Causes the instrument to enter a state where the front panel keys are inoperative. In this state, the instrument will only accept parameter changes through the remote interfaces. To enable front panel parameter changes, the GPIB controller can send the GTL (Go To Local) command (see paragraph 3.4).

Addressed Commands

Addressed commands are used to command a device to perform designated actions. Addressed commands are recognized only when the instrument is addressed as a *listener*. Addressed commands performed by the instrument are:

1. Go To Local (GTL) — Commands the instrument to enable front panel control.
2. Selective Device Clear (SDC) — Resets the instrument to its power on default conditions. SDC affects only the selected unit.
3. Group Execute Trigger (GET) — Upon receipt of the GET, the programmed settings located in scratchpad are transferred to the operational section of the instrument as if an execute ('I') command had been

sent. The execute command is described in paragraph 3.4.1.7.

3.4.1.4 Listen Always Mode

The Listen Always (Listen Only) mode may be selected when the application does not require addressing individual listeners. In this mode, the device is automatically addressed as a listener and is ready to receive bus messages whenever the REN line goes true. Setting this switch on the Model 552A or 553A is described in paragraph 2.3.3.2.

3.4.1.5 Characters

There are four types of characters that can be sent over the GPIB bus. These are:

Alphabetic characters: A, C, D, F, H, I, L, M, O, S and T select filter or control commands. Both upper and lower case characters are treated identically. All other alphabetic characters except 'E' (considered a numeric character) are ignored.

Numeric characters: Numbers 0 through 9, E (exponent), − (negative), + (positive) and the decimal point determine the parameter value or control code.

Terminators: 'CR' (carriage return), 'LF' (line feed) or assertion of EOI (GPIB only) terminates a character string. One or more of these terminators must follow all incoming strings. When transmitting, the instrument always sends 'CR', 'LF' and 'EOI' as the terminator.

Nonprogramming characters: Any character not previously described is ignored and may be interspersed freely after any programming character.

3.4.1.6 Parameter Commands

The only types of parameter commands possible on the Models 552A and 553A are filter and control commands.

Filter parameter commands set values such as cutoff frequency and input sensitivity for the filter and gain stages. They are buffered in scratchpad memory when received, then directed to the operational sections of the instrument when executed with an 'I' command. Multiple commands may be sent in the same string. For example, to simultaneously program cutoff frequency to 10 kHz and input sensitivity to −10 dBV, send the parameter string 'F10E3S-10I'.

Control parameter commands set the interface programming mode and function as soon as they are received and processed. They bypass the scratchpad memory and do not require an execute ('I') command.

3.4.1.7 The Execute Command ('I')

The execute command ('I') makes possible a wide variety of programming options. By excluding 'I' from a program string, new filter parameters are entered into scratchpad memory only. If there are no class 2 errors (see paragraph 3.4.1.8), these parameters are then transferred from scratchpad memory to the operational control registers when 'I' is sent over the bus, either alone or at the end of a string. When 'I' is included at the end of a string, the parameters in that string are entered into scratchpad memory and transferred, along with the remaining scratchpad contents, to the operational control registers.

3.4.1.8 Errors

After the instrument receives a terminator, the string is processed to remove any non-programming characters (see paragraph 3.4.1.5). Each parameter value is then truncated to an integer and verified as a legal value.

If a frequency value with more than two digits of resolution is sent, the excess digits are simply deleted with no error being generated.

Class 1 Errors—Out of Range: Class 1 errors are caused by programming values outside the legal limits (shown in table 3-1) of the selected parameter. For example, programming a cutoff frequency of 100000 Hz will cause a class 1 frequency error (since 50000 is the highest valid frequency setting). When this occurs, the instrument disregards the new value and retains the previously programmed value in scratchpad memory. The error is recorded in the error string and may be examined on request. Sending a 'D' command to channel 1 of the Model 553A will cause a class 1 error. See talk mode 'T0' in table 3-2.

Table 3-1. Class 1 Error Guidelines

Parameter	Legal Truncated Integer Value
Frequency (F)	10 to 50000
Input Sensitivity (S)	−60 to +20
Output Gain (O)	0 to 10
Channel Select (C)	1 to 3
Talk Mode (T)	0 to 6
Local Mode (L)	0 to 1
Handshake (H)	0 to 3
Interrupt Mask (M)	0 to 255

Class 2 Errors — Conflict Between Parameters: A class 2 error is initiated when two programmed parameters conflict. The only class 2 error for this instrument occurs

when dc coupling is selected for full scale input sensitivities from −40 to −60 dBV. If this conflict exists, ac coupling is forced into the scratchpad and the error is recorded in the error list.

Class 3 Errors — Parameter Needs Adjustment: As previously explained, programmed strings are first integer truncated, then tested for class 1 errors. After completion of these first two steps, input sensitivity and output gain parameters are adjusted, if necessary, to the nearest value which the instrument can execute. If adjustment is made, the scratchpad memory is loaded with the adjusted value and a class 3 error is reported in the error string buffer.

Input sensitivity is adjusted to the next more positive (less sensitive) 5 dB step value to avoid computed gain value overload problems. For example, programmed values of 'S-31' and 'S-34' would be adjusted to 'S-30', (−30 dBV full scale). Input sensitivity is never adjusted to a more negative (more sensitive) value. The output gain is adjusted to either 0 dB or 10 dB, whichever is closest to the programmed value.

3.4.1.9 Programming Parameters

Filter and control parameter commands require an alphabetic letter, usually followed by a number value.

Only one decimal point and one 'E' (exponent) are allowed per number, all others are ignored. Only two exponent digits are allowed. Any number of nonprogramming characters may be interspersed with the numeric field as they have no effect.

Data entry can be fixed point, floating point, exponential notation for scientific notation. Any sequence of characters (except in-line math such as '5-2' to arrive at '3') which gives the new value is acceptable. For example, all of the following sequences cause frequency 100 Hz to be programmed.

Programming String For Frequency 100 Hz	Remarks
F 100	Blank spaces are ignored
F0100	Leading zeros are ignored
F1E2	$1*10^2 = 100$
F.01E4	$.01*10^4 = 100$
F.01E304	$.01*10^4 = 100$ Last two exponent digits are only used
F1000E-1	$1000*10^{-1} = 100$
F1E-2-	Two minus signs cancel
F1E.2	Decimal point in exponent is ignored

Since the numeric input format is so general, the instrument must be told when to terminate the numeric field so it can evaluate the number. This is done by programming either a legal alphabetic character specifying the next parameter field (non-programming characters are not sufficient) or a terminator. After terminating the numeric field, the new value is integer truncated and verified to be within range. If it is not within range, an error string is generated and the previous value is retained.

3.4.1.10 Talk Mode

The talk mode command enables the instrument to send several different parameter and status messages to the controller if the unit is addressed as a talker.

The description of each command message is given in table 3-2. Only error messages (T0, T1 or T6) are cleared immediately after being sent. All others remain until cleared by the instrument.

3.4.1.11 Service Request (SRQ) Interrupts

The instrument is capable of alerting the controller of an error condition by using the service request (SRQ) line.

Several types of errors are detected in the instrument. The user can specify which errors are to cause an SRQ. Each error condition is 'enabled' by sending the appropriate error weight using the interrupt mask command. The format command is the letter 'M' followed by a decimal number representing the sum of the weights in the following chart.

Decimal Weight	Error Type
128	Address Pass Through Error
64	Not Used
32	Buffer Overflow
16	Channel 2 Overload
8	Channel 1 Overload
4	Class 3 Error
2	Class 2 Error
1	Class 1 Error

NOTE

The interrupt mask ('M') numeric format must be entered in integer form using no decimal point or exponent.

If any of the above error weights are included in the interrupt mask, an SRQ interrupt is generated when that error condition occurs. For example, if the user requires an SRQ for a buffer overflow, an overload on channel 2 or a class 1 programming error, the interrupt mask

number (sum of the weights) would be decimal 49 (32 + 16 + 1). The program string would be 'M49'. To disable all SRQ interrupt error sources, send the string 'M0'.

When an enabled error occurs, the SRQ line is set true, and, in the serial poll byte, the bit corresponding to the error and the rsv bit are both set to one. These bits remain set until the serial poll byte is read, either by addressing the device as a talker when in talk mode T1 or by issuing a Serial Poll Enable (SPE) sequence. Either of these clears all error bits in the serial poll byte and releases the SRQ line on the bus.

As errors are detected, the corresponding bits in the serial poll byte are set. The serial poll byte thus represents the accumulated error history since the last time the byte was read and cleared. Note that all errors are recorded in the serial poll byte, not just those enabled with the 'M' command. However, only those errors which are enabled will cause an SRQ.

If the user wishes to know the error history, the serial poll byte may be read at any time using an SPE sequence or talk mode T1.

NOTE

Programming changes may cause momentary switching transients leading to a false overload indication (interrupt weight 8 or 16). If a transient causes an overload, the error bit in the serial poll byte will be cleared when read by the controller. If the overload is sustained, after the serial poll byte is read and the error bit cleared, the bit will again be set. In this case, however, a second SRQ will not be generated until after the next 'I' command is sent. This avoids a "race" condition, where the controller is constantly servicing the SRQ interrupts.

3.4.1.12 GPIB Programming Reference Guides

Tables 3-2 and 3-3 can be used as programming reference guides when writing GPIB statements to the Model 552A or 553A. They describe each programming command and which numeric characters are to be used to program parameter values. Table 3-2 describes control parameters and table 3-3 describes filter parameters. Before attempting to use this guide, read paragraphs 3.4.1 through 3.4.1.11.

Table 3-2. GPIB Control Parameter Programming Reference Guide

Function	ASCII Character	Description
Channel Select	C	The character 'C' followed by a single digit code between 1 and 3 selects which channel(s) will be affected by subsequent programming parameters. **Channel** — **Code** Channel 1 only — C1 Channel 2 only — C2 Both Channels 1 and 2 — C3
Execute	I	Causes the scratchpad contents to be transferred to the active parameter table and executed. An execute ('I') may be sent as the last character in the parameter string if the new parameter is to be executed immediately.
Interrupt Mask	M	The character 'M' followed by a number ('0' to '255') sent from the controller to the Model 552A or 553A selects the condition(s) that will cause the instrument to interrupt the GPIB bus. The number is the sum of the ASCII decimal weights of the error types listed below, selected individually or in any combination. Decimal weights representing nonselected errors are "masked" or "false" in the 8 bit binary code. Weight 64 has no effect if selected. All SRQ interrupt error types may be disabled by sending the string 'MO'.

Table 3-2. GPIB Control Parameter Programming Reference Guide (Continued)

Function	ASCII Character	Description
Interrupt Mask (Cont)	M	**Decimal Weight** / **Error Type** 128 Address Pass Through Error 64 Not Used 32 Buffer Overflow 16 Channel 2 Overload 8 Channel 1 Overload 4 Class 3 Error 2 Class 2 Error 1 Class 1 Error
Talk Mode	T	The character 'T' followed by a code (0 through 6) selects the kind of message the instrument will send when it is addressed as a talker on the GPIB. To read a message from the instrument, send the talk address (with ATN on) over the bus. The instrument will then send the message currently selected by the Talk Mode ('T') setting. All messages are sent in ASCII format with numbers in decimal form. The last character will be 'CR' + 'LF' with the EOI line asserted. **Code** / **Message** T0 Programming error list. A typical error string is 'E 1F 2DS'. Some error string characteristics are: A. All error strings begin with 'E'. B. Most recent error is at the end of the string. C. Errors are separated by space. D. Class 1 error: A '1' followed by the programming character that caused the error (example '1F'). E. Class 2 error: A '2' followed by 'DS' since dc coupling (D) and sensitivity (S) are the only two possible conflicting parameters. F. Error strings can be up to 80 characters in length (including spaces). G. After transfer, the error string is cleared. T1 Serial poll byte response: The serial poll status byte is converted to an ASCII decimal number between '0' and '255'. After the string is sent, the serial poll status byte is cleared to all zeros and the SRQ line is released. T2 The most recently programmed parameter string is sent. T3 The entire instrument setup after last execute. Example: 'C1 F12000 S-60 O00 A C2 F300 S-00 O10 D M008 H2 T3 L1 C1', where 'C' designates channel A (1) or B (2), 'F' is the cutoff frequency in Hz, 'S' is full scale sensitivity in dBV, 'O' is output gain in dB and coupling is shown as 'A' (ac) or 'D' (dc). Following the conditions for the second channel, 'M' is the interrupt mask, 'H' is the handshake mode, 'T' is the talk mode and 'L' is the local (front panel) control mode. The final 'C' indicates the selected channel(s) for subsequent programming.

NOTE

The T3 string can be stored and later programmed into the instrument to restore the same configuration.

Table 3-2. GPIB Control Parameter Programming Reference Guide (Continued)

Function	ASCII Character	Description
Talk Mode (Cont)	T	T4 All filter parameter scratchpad values that will be executed when the next 'I' is received. Same format as T3 except that only C, F, S, O, A and D parameters are included. T5 Instrument identification and software version. Example: 'Wavetek Model 552A (or 553A) REV C'. T6 RS-232-C UART Status: The UART (Universal Asynchronous Receiver/ Transmitter) for the RS-232-C port can report its error status with an ASCII decimal number between 0 and 7 according to the following list. **Weight** **Error** 4 Framing Error 2 Parity Error 1 Overrun Error The status is cleared after being read. This mode is provided for applications where both GPIB and RS-232-C interfaces are used alternately.
Exponent	E	The character 'E' and optional +/− entries allow using the power of 10 to enter numeric values. For example, 'F300E-1' = Frequency $300*10^{-1}$ = Frequency 30Hz.
Local Control	L	The character 'L' followed by a single digit code selects front panel keys enabled ('L1') or disabled ('L0') during remote control operation. The power up default condition is 'L1'. 'L1' and 'L0' are NOT equivalent to the GPIB universal commands 'LL0' and 'GTL'.
Handshake	H	The character 'H' followed by a single digit code between 0 and 3 allows alteration of the RS-232-C interface software and hardware handshake protocols described in paragraph 3.4.2.4. **RTS/CTS (Hardware)** **XON/XOFF (Software)** **Code** Off Off H0 On Off H1 Off On H2 On On H3 The power up default condition is 'H0'. This mode is provided for applications where both GPIB and RS-232-C interfaces are used alternately.

Table 3-3. GPIB Filter Parameter Programming Reference Guide

Function	ASCII Character	Description
Input Coupling	A	The character 'A' (not followed by a numeral) selects ac input coupling.
	D	The character 'D' (not followed by a numeral) selects dc input coupling. This is not allowed for Model 553A channel 1.
Cutoff Frequency	F	The character 'F' followed by a number value between '10' and '50000' programs the filter cutoff frequency in hertz for the selected channel(s).
Output Gain	O	The character 'O' followed by a number value of either '0' or '10' programs the post-filter output gain in dB for the selected channel(s).
Input Sensitivity	S	The character 'S' followed by a number value between ' − 60' and ' + 20' (in 5 dB increments) programs the full scale input sensitivity of the selected channel(s) in dBV. 0 dBV equals 1 Vrms.

3.4.2 RS-232-C Interface

3.4.2.1 Initial Preparations

Connect the controller to the instrument RS-232-C rear panel connector as described in paragraphs 2.3.4.1 and 2.3.4.3.

Set the rear panel RS-232-C switches (described in paragraph 2.3.4.2) to match the parameters of the controller. In general, the highest available baud rate should be used to minimize message transmission time.

3.4.2.2 General RS-232-C Information

RS-232-C Voltage Levels

Data signal lines TxD and RxD use a voltage of + 3 to + 25V to represent a zero (also called a space) and a voltage of − 3 to − 25V to represent a one (also called a mark). Control signal lines (RTS, CTS, etc.) use + 3 to + 25V to indicate a true condition and − 3 to − 25V to indicate a false condition. Active mode lines DSR and DTR (paragraph 3.4.2.3) also use + 3 to + 25V and − 3 to − 25V to indicate their conditions.

Data Transmission

When no data is being transmitted, the idle state of the data lines will be the mark state (low). To transmit a byte, the transmitting device first sends a start bit which is a space for one bit time (1/baud rate) to synchronize the receiver. The next 7 or 8 data bits are sent LSB first, then at least one bit time of the mark state (stop bit) before initiating the transmission of the next byte. The baud rate and the number of stop and data bits is selectable by using the rear panel dip switch located next to the RS-232-C connector.

To verify proper transmission of data, some devices send an optional parity bit between the data bits and stop bit. Even or odd parity is possible and must be selected according to the system requirements. When even parity is selected, the parity bit is set to '1' when the number of 1's in the data field is odd, and to '0' when the number of 1's in the data field is even. When odd parity is selected, the parity bit is set to '1' when the number of 1's in the data field is even, and to '0' when the number of 1's in the data field is odd. Selection of parity and the odd/even state is accomplished by using the rear panel dip switch located next to the RS-232-C connector.

3.4.2.3 Initiating RS-232-C Control

The only actions which initiate the RS-232-C active mode are a low-to-high transition on the DTR input line or the serial control character '!' being sent on the RxD line. The instrument acknowledges the RS-232-C active mode being enabled by sending DSR high.

To disable the RS-232-C active mode, the controller must send either a high-to-low transition on the DTR line, or the serial control character '$' on the RxD line. This causes the instrument to bring the DSR line low, and may be used by the controller to verify successful transition into or out of the RS-232-C active mode.

RS-232-C Priority Over GPIB

The RS-232-C mode has priority over the GPIB mode. Either a low-to-high transition on the DTR line, or the receipt of a '!' on the RS-232-C port while the GPIB mode is active will abort the GPIB mode, reset any active LISTEN or TALK state and enable the RS-232-C active mode. Disabling the RS-232-C active mode does not re-establish the GPIB active mode.

CAUTION

If the DTR line is changed during any GPIB or RS-232-C data transfer, unpredictable results may occur.

3.4.2.4 Handshake System

A bidirectional handshake system is used in the Model 552A and 553A to help prevent loss of transmitted data. At any given moment, either the instrument or the controller can assume transmitter or receiver status. When the transmitter sends data faster than it can be accepted by the receiver, it signals the transmitter to wait until the previously transmitted data is processed.

Both software and hardware handshaking are provided. Software handshaking involves sending 'XON' and 'XOFF' characters to indicate the receiving device status. Hardware handshaking uses the RTS and CTS lines to indicate receiver status. Depending on the system requirements, either, both, or neither of these methods may be required.

Software Handshake (XON/XOFF)

The XON/XOFF protocol system, which is disabled at power on, is controlled by the 'H' command as shown in table 3-6. This system employs two serial control characters 'XON' ($11) and 'XOFF' ($13). When the receiver is unable to process any more data, it sends the 'XOFF' character to the transmitter. The 'XON' character is sent when the receiver is again ready to accept data.

Since the transmitter requires time to process the 'XOFF' character, some data may be sent after an 'XOFF' is received. Because of this, when the Model 552A or 553A is transmitting data, it will send no more than three characters after receiving an 'XOFF'. When acting as a receiver, the instrument sends 'XOFF' each time a command line terminator character is received and 'XON' after the command line is processed.

NOTE

To prevent losing characters after the controller has transmitted a terminator character, additional command characters MUST NOT be sent to the instrument until 'XOFF' followed by 'XON' has been transmitted.

Once the 'H' command has enabled the XON/XOFF system, the instrument will continue to transmit 'XON' and 'XOFF' to the controller under all conditions, including pending 'XOFF' or RTS holdoffs by the controller.

Hardware Handshake (RTS/CTS)

The RTS and CTS lines provide hardware handshaking for the Model 552A and 553A. This feature is disabled at power on, but may be enabled or disabled by using the remote 'H' command as shown in table 3-6. The RTS line is driven by the controller, while the instrument drives the CTS line.

If the instrument is in the transmit mode, a high on the RTS line enables data transmission, while a low disables transmission. When the controller is unable to process any more data, it pulls the RTS line low, preventing the instrument from transmitting more than three additional characters. The RTS line is returned high when the controller is again ready to accept data.

With the controller sending data, a high on the CTS line enables transmission, while a low disables transmission. When the instrument receives a terminator character, it pulls the CTS line low, preventing the controller from transmitting. After processing the command line, the instrument returns the CTS line high.

NOTE

To prevent losing characters after the controller has transmitted a terminator character, additional command characters MUST NOT be sent to the Model 552A or 553A until the CTS line has been brought low, then returned high.

No Handshake

When transmitting to the controller, Models 552A and 553A send data without waiting. If the controller cannot receive the data fast enough, data will be lost. To reduce the data rate (characters per second) from the instrument, the baud rate setting can be reduced to the point where the controller can keep up with the instrument.

When receiving data from the controller, the instrument will accept data at any baud rate up to the point where it receives a terminator. At this time, the controller must stop sending data for one second for each 'I' command in the preceding command string.

3.4.2.5 Characters

There are five types of characters that can be sent over the RS-232-C serial interface. These are:

Alphabetic characters. A, C, D, F, H, I, L, M, O, S and T select filter or control commands. Both upper and lower case characters are treated identically. All other alphabetic characters except 'E' (considered a numeric character) are ignored.

Numeric characters. Numbers 0 through 9, E (exponent), – (negative), + (positive) and the decimal point determine the parameter value or control code.

Interface control characters. Characters '!', '$', '?', 'XON' and 'XOFF' are reserved for special functions.

Terminators. 'CR' (carriage return) or 'LF' (line feed) terminate a character string. One or both of these terminators may follow incoming strings. When transmitting, the instrument always sends both 'CR' and 'LF' as a terminator.

Nonprogramming characters. Any character not previously described is ignored and may be interspersed freely after any programming character.

3.4.2.6 Parameter Commands

The only types of parameter commands possible on the Model 552A and 553A are filter and control commands.

Filter parameter commands set values such as cutoff frequency and input sensitivity for the filter and gain stages. They are buffered in scratchpad memory when received, then directed to the operational sections of the instrument when executed with an 'I' command. Multiple commands may be sent in the same string. For example, to simultaneously program cutoff frequency to 10 kHz and input sensitivity to – 10 dBV, send the parameter string 'F10E3S-10I'.

Control parameter commands set the interface programming mode and function as soon as they are received and processed. They bypass the scratchpad memory and do not require an execute ('I') command.

3.4.2.7 The Execute Command ('I')

The execute command ('I') makes possible a wide variety of programming options. By excluding 'I' from a program string, new parameters are entered into scratchpad memory only. These parameters are then transferred to the operational control registers when 'I' is sent, either alone or at the end of a string. When 'I' is included at the end of a string, the parameters in that string are entered into scratchpad memory and transferred, along with the remaining scratchpad contents, to the operational control registers.

3.4.2.8 Errors

When the instrument receives data, each parameter value is rounded to the nearest integer and verified as a legal value.

Class 1 Errors — Out of Range: Class 1 errors are caused by programming values outside the legal limits (shown in table 3-4) of the selected parameter. For example, programming a cutoff frequency of 100,000 kHz will cause a class 1 frequency error (since 50000 is the highest valid frequency setting). When this occurs, the instrument disregards the new value and retains the previously programmed value in scratchpad memory. The error is recorded in the error string and may be examined on request. Sending a 'D' command to channel 1 of the Model 553A will cause a class 1 error. See talk mode T0 in table 3-6.

Table 3-4. Class 1 Error Guidelines

Parameter	Legal Truncated Integer Value
Frequency (F)	10 to 50000
Input Sensitivity (S)	– 60 to + 20
Output Gain (O)	0 to 10
Channel Select (C)	1 to 3
Overload Enable (V)	0 to 1
Talk Mode (XT)	0 to 5
Local Mode (L)	0 to 1
Handshake (H)	0 to 3

Class 2 Errors — Conflict Between Parameters: A class 2 error is initiated when two programmed parameters conflict. The only class 2 error for this instrument occurs when dc coupling is selected for full scale input sensitivities from – 40 to – 60 dBV. If this conflict exists, ac coupling is forced into the scratchpad and the error is recorded in the error list.

Class 3 Errors — Parameter Needs Adjustment: As previously explained, programmed strings are first integer truncated, then tested for class 1 errors. After completion of these first two steps, input sensitivity and output gain parameters are adjusted, if necessary, to the nearest value which the instrument can execute. If adjustment is made, the scratchpad memory is loaded with the adjusted value and a class 3 error is reported in the error string buffer.

Input sensitivity is adjusted to the next more positive (less sensitive) 5 dB step value to avoid computed gain value overload problems. For example, programmed values of 'S-31' and 'S-34' would be adjusted to 'S-30', (– 30 dBV full scale). Input sensitivity is never adjusted to a more negative (more sensitive) value. The output gain is adjusted to either 0 dB or 10 dB, whichever is closest to the programmed value.

3.4.2.9 Programming Parameters

Filter and control parameter commands require an alphabetic letter, usually followed by a number value.

Only one decimal point and one 'E' (exponent) are allowed per number, all others are ignored. Only two exponent digits are allowed. Any number of nonprogramming characters may be interspersed with the numeric field as they have no effect.

Data entry can be fixed point, floating point, exponential notation or scientific notation. Any sequence of characters which gives the new value is acceptable. For example, all of the following sequences cause frequency 100 Hz to be programmed.

Programming String For Frequency 100 Hz	Remarks
F 100	Blank spaces are ignored
F0100	Leading zeros are ignored
F1E2	$1*10^2 = 100$
F.01E4	$.01*10^4 = 100$
F.01E304	$.01*10^4 = 100$ Last two exponent digits are only used
F1000E-1	$1000*10^{-1} = 100$
F1E-2-	Two minus signs cancel
F1E.2	Decimal point in exponent is ignored

Since the numeric input format is so general, the instrument must be told when to terminate the numeric field so it can evaluate the number. This is done by programming either an alphabetic character or a terminator. After terminating the numeric field, the new value is rounded and verified to be within range. If it is not within range, an error string is generated and the previous value is retained.

3.4.2.10 Talk Mode

The talk mode command enables the instrument to send several different parameter and status messages back to the controller. The controller must first send the interface control character '?' before a message can be sent.

The description of each command message is given in table 3-6. Only error messages (T0, T1 or T6) are cleared immediately after being sent. All others remain until cleared by the instrument.

3.4.2.11 Interrupts

The instrument is capable of alerting the controller of an error condition by using the interrupt system. The interrupt sequence consists of sending the escape character 'ESC', carriage return 'CR' and line feed 'LF' on the TxD line.

Several types of errors are detected in the instrument. The user can specify which errors are to cause an interrupt. Each error condition is 'enabled' by sending the appropriate error weight using the interrupt mask command. The format for this command is the letter 'M' followed by a decimal number representing the sum of the weights in the following chart.

Decimal Weight	Error Type
128	RS-232-C UART Error
64	Not Used
32	Buffer Overflow
16	Channel 2 Overload
8	Channel 1 Overload
4	Class 3 Error
2	Class 2 Error
1	Class 1 Error

NOTE

The interrupt mask ('M') numeric format must be entered in integer form using no decimal point or exponent.

If any of the above error weights are included in the interrupt mask, an interrupt is generated when that error condition occurs. For example, if the user requires an interrupt for a buffer overflow, an overload on channel 2 or a class 1 programming error, the interrupt mask number (sum of the weights) would be decimal 49 (32 + 16 + 1). The program string would be 'M49'. To disable all interrupt error sources, send the string 'M0'. When the UART error is included, an overrun, framing or parity error will cause an interrupt.

When an enabled error occurs, the interrupt sequence ('ESC' + 'CR' + 'LF') is sent, and the bit in the serial poll byte corresponding to the error is set to one. The bit remains set until the serial poll byte is read using talk mode T1 (see paragraph 3.4.2.10).

As errors are detected, the corresponding bits in the serial poll byte are set. The serial poll byte thus represents the accumulated error history since the last time the byte was read and cleared. Note that all errors are recorded in the serial poll byte, not just those enabled

with the 'M' command. However, only those errors which are enabled will cause an interrupt.

If the user wishes to know the error history, the serial poll byte may be read at any time using talk mode T1.

NOTE

Programming changes may cause momentary switching transients leading to a false overload indication (interrupt weight 8 or 16). If a transient causes an overload, the error bit in the serial poll byte will be cleared when read by the controller. If the overload is sustained, after the serial poll byte is read and the error bit cleared, the bit will again be set. In this case, however, a second interrupt will not be generated until after the next 'I' command is sent. This avoids a "race" condition, where the controller is constantly servicing the interrupts.

3.4.2.12 RS-232-C Programming Reference Guides

Tables 3-5, 3-6 and 3-7 can be used as programming reference guides when writing RS-232-C statements to the Model 552A or 553A. They describe each programming command and which numeric characters are to be used to program parameter values. Table 3-5 describes RS-232-C interface control characters, table 3-6 describes RS-232-C control parameter programming and table 3-7 describes RS-232-C filter parameter programming. Before attempting to use this guide, read paragraphs 3.4.2.1 through 3.4.2.11.

Table 3-5. RS-232-C Interface Control Character Reference Guide

Character	ASCII (Hex)	Function
!	21	Causes the instrument to enter the RS-232-C active mode, sending the DSR line high. Receiving '!' is equivalent to a low-to-high transition of the DTR line. The RS-232-C active mode can be exited by sending '$' or bringing the DTR line low.
$	24	Causes the instrument to leave the RS-232-C active mode, sending the DSR line low. All subsequent RS-232-C interface signals except '!' or a low-to-high transition of the DTR line are ignored.
?	3F	Causes the instrument to send the talk message designated by the talk mode as explained in paragraph 3.4.2.10. and table 3-6.
XOFF	13	Causes the instrument to stop transmitting data only if the XON/XOFF protocol is enabled.
XON	11	Cancels the XOFF condition, allowing transmission of data to resume.

Table 3-6. RS-232-C Control Parameter Programming Reference Guide

Function	ASCII Character	Description
Channel Select	C	The character 'C' followed by a single digit code between '1' and '3' selects which channel(s) will be affected by subsequent programming parameters. **Channel** — **Code** Channel 1 only — C1 Channel 2 only — C2 Both Channels 1 and 2 — C3
Execute	I	Causes the scratchpad contents to be transferred to the active parameter table and executed. An execute ('I') may be sent as the last character in the parameter string if the new parameter is to be executed immediately.
Interrupt Mask	M	The character 'M' followed by a number ('0' to '255') sent from the controller to the Model 552A or 553A selects the condition(s) that will cause the instrument to interrupt the RS-232-C interface. The number is the sum of the ASCII decimal weights of the error types listed below, selected individually or in any combination. Decimal weights representing nonselected errors are "masked" or "false" in the 8 bit binary code. Weight 64 has no effect if selected. All interrupt error types may be disabled by sending the string 'MO'. **Decimal Weight** — **Error Type** 128 — RS-232-C UART Error 64 — Not Used 32 — Buffer Overflow 16 — Channel 2 Overload 8 — Channel 1 Overload 4 — Class 3 Error 2 — Class 2 Error 1 — Class 1 Error
Talk Mode	T	The character 'T' followed by a code ('0' through '6') selects the kind of message the instrument will send when requested. All messages are sent in ASCII format with numbers in decimal form followed by 'CR' + 'LF'. **Code** — **Message** T0 — Programming error list. A typical error string is 'E 1F 2DS'. Some error string characteristics are: A. All error strings begin with 'E'. B. Most recent error is at the end of the string. C. Errors are separated by space. D. Class 1 error: A '1' followed by the programming character that caused the error (example '1F'). E. Class 2 error: A '2' followed by 'DS' since dc coupling (D) and sensitivity (S) are the only two possible conflicting parameters. F. Error strings can be up to 80 characters in length (including spaces). G. After transfer, the error string is cleared.

Table 3-6. RS-232-C Control Parameter Programming Reference Guide (Continued)

Function	ASCII Character	Description	
Talk Mode (Cont)	T	T1	Serial poll byte response: The serial poll status byte is converted to an ASCII decimal number between '1' and '255'. After the string is sent, the serial poll status byte is cleared to all zeros. If the error condition is removed, the bit will still remain latched until the byte is read.
		T2	The most recently programmed parameter string is sent. All RS-232-C interface control characters are removed from the string.
		T3	The entire instrument setup after last execute. Example: 'C1 F12000 S-60 O00 A C2 F300 S-00 O10 D M008 H2 T3 L1 C1', where 'C' designates channel A (1) or B (2), 'F' is the cutoff frequency in Hz, 'S' is full scale sensitivity in dBV, 'O' is output gain in dB and coupling is shown as 'A' (ac) or 'D' (dc). Following the conditions for the second channel, 'M' is the interrupt mask, 'H' is the handshake mode, 'T' is the talk mode and 'L' is the local (front panel) control mode. The final 'C' indicates the selected channel(s) for subsequent programming.

NOTE

The T3 string can be stored and later programmed into the instrument to restore the same configuration.

		T4	All filter parameter scratchpad values that will be executed when the next 'I' is received. Same format as T3 except that only C, F, S, O, A and D parameters are included.
		T5	Instrument identification and software version. Example: 'Wavetek Model 552A (or 553A) REV C'.
		T6	RS-232-C UART Status: The UART (Universal Asynchronous Receiver/ Transmitter) for the RS-232-C port can report its error status with an ASCII decimal number between '0' and '7' according to the following list.

Weight	Error
4	Framing Error
2	Parity Error
1	Overrun Error

Exponent	E	The character 'E' and optional +/- entries allow using the power of 10 to enter numeric values. For example, 'F300E-1' = Frequency $300*10^{-1}$ = Frequency 30Hz.
Local Control	L	The character 'L' followed by a single digit code selects front panel keys enabled ('L1') or disabled ('L0') during remote control operation. The power up default condition is 'L1'.

Table 3-6. RS-232-C Control Parameter Programming Reference Guide (Continued)

Function	ASCII Character	Description
Handshake	H	The character 'H' followed by a single digit code between 0 and 3 allows alteration of the software and hardware handshake protocols described in paragraph 3.4.2.4. **RTS/CTS (Hardware) / XON/XOFF (Software) / Code** Off / Off / H0 On / Off / H1 Off / On / H2 On / On / H3 The power up default condition is 'H0'. Disabling XON/XOFF protocol will clear an existing XOFF condition.

Table 3-7. RS-232-C Filter Parameter Programming Reference Guide

Function	ASCII Character	Description
Input Coupling	A	The character 'A' (not followed by a numeral) selects ac input coupling.
	D	The character 'D' (not followed by a numeral) selects dc input coupling. This is not allowed for Model 553A channel 1.
Cutoff Frequency	F	The character 'F' followed by a number value between '10' and '50000' programs the filter cutoff frequency in hertz for the selected channel(s).
Output Gain	O	The character 'O' followed by a number value of either '0' or '10' programs the post-filter output gain in dB for the selected channel(s).
Input Sensitivity	S	The character 'S' followed by a number value between '−60' and '+20' in 5 dB increments programs the full scale input sensitivity of the selected channel(s) in dBV. 0 dBV equals 1 Vrms.

SECTION 4
CIRCUIT DESCRIPTION

4.1 INTRODUCTION

Figure 4-1 is a block diagram of the Model 552A or 553A Dual Channel Programmable Filter. The Z80 microprocessor and amplifier/filter control sections determine the status of the analog circuitry, front panel displays and remote operation LEDs. The microprocessor receives manual instructions from the front panel keyboard or remote instructions from the IEEE-488 bus and RS-232-C interface. The front panel keyboard is always overridden by either remote interface, but the RS-232-C has top priority as explained in paragraph 3.4.

The attenuator/amplifier circuit accepts input signals from J5 (J7 for channel 2) and provides up to 20 dB of attenuation or 60 dB of gain in 5 dB steps as determined by the programmed full scale amplitude. The microprocessor selects the appropriate combination of attenuation and/or amplification to obtain the desired output level. Isolation between digital control and analog signal grounds is accomplished through relays and optoisolators. The attenuator/amplifier output signal drives the overload sense and filter circuits.

The overload sense circuit alerts the microprocessor of an excessively positive or negative voltage at the attenuator/amplifier circuit output. If an overload occurs, the front panel flashes OVLD on the appropriate channel and, if not masked out (see paragraph 3.4.1.11 for IEEE-488 and paragraph 3.4.2.11 for RS-232-C), an interrupt is sent over the enabled interface. Short duration overload pulses are detected by a pulse stretcher within the overload sense circuit.

Both channels on the Model 552A and channel 2 on the Model 553A use three stage elliptic low pass filters to produce a relatively flat response at and below the programmed cutoff frequency, then a sharp drop in amplitude in the stopband. At two frequency locations above cutoff, sharp drops in amplitude (transmission nulls) pull the filter output below − 80 dB. Other filtering components maintain the remaining frequencies below − 72 dB. The programmed frequency determines the status of digital lines from the microprocessor circuitry that control the turning on or off of FETs and relays that connect precision components used in the filter.

Channel 1 of the Model 553A uses a three stage elliptic high pass filter to provide − 72 dB of attenuation in the stopband, then a sharp increase in amplitude as the signal frequency approaches the programmed cutoff frequency followed by a relatively flat response in the passband (up to 300 kHz). At two frequency locations below cutoff, sharp drops in amplitude called "transmission nulls" pull the filter output below − 80 dB. Other filtering components maintain the remaining frequencies below − 72 dB. The programmed frequency determines the status of digital lines from the microprocessor circuitry that control the turning on or off of FETs and relays that connect precision components used in the filter.

4.2 MAINBOARD

4.2.1 Attenuator/Amplifier

Refer to schematic 0103-00-2364 sheet 1 of 5 for Model 552A, 0103-00-2872 for Model 553A. Except for component designators and load enable (LE) lines, Model 552A circuitry in channel 1 and channel 2 is identical. Only channel 1 is discussed. For Model 553A, circuit differences are discussed in text.

Input signals at J5 pass through C1 for ac coupling (K1 contacts open) or R1 (not included in Model 553A channel 1) for dc coupling (K1 contacts closed) to an attenuator tree providing 0, 20 or 40 dB of attenuation. For 0 attenuation, all K3 and K4 relay contacts are open, and both sets of K2 contacts are closed. The input signal is connected directly to the left end of R6 and the required 1 MΩ input impedance to ground is provided through R14. For 20 dB of attenuation, all K2 and K4 relay contacts are open, and both sets of K3 contacts are closed. The bottom of R5 and C5 are shorted to ground, and the junction of R4 and R5 is connected to the left end of R6. Voltage divider R4 and R5 provide the selected amount of signal attenuation as well as the 1 MΩ input impedance to ground. High frequency compensation is provided by C4. For 40 dB of attenuation, all K2 and K3 relay contacts are open, and both sets of K4 contacts are closed. The bottom of R3 and C3 are shorted to ground, and the junction of R2 and R3 connect to the left end of R6. The required attenuation is accomplished with voltage divider R2 and R3, which also provides the 1 MΩ

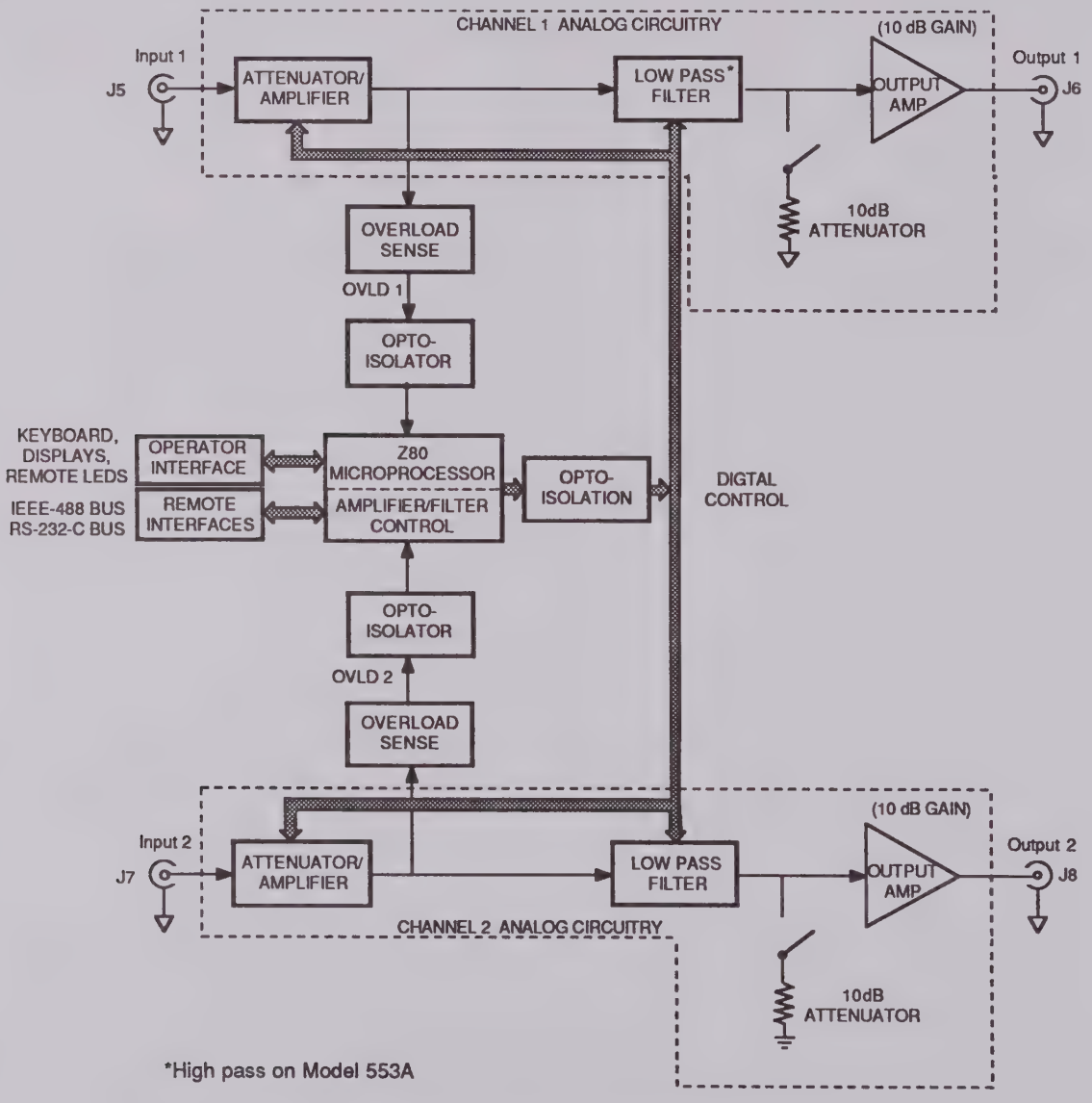


Figure 4-1. Model 552A/553A Simplified Block Diagram

input impedance to ground. High frequency compensation is adjusted with C2. Table 5-21 shows the status of relays K2, K3 and K4 to obtain the proper attenuation for the selected full scale sensitivity.

Data lines D0 through D3 determine the state of relays K1 through K4 when LE5 (at quad latch U9 pin 9) is high. Hex peripheral driver U1 provides the current needed to power these relays. Isolation between digital and signal grounds is accomplished through the relays.

Overvoltage protection is provided by CR1, CR2, CR119, CR120, R6, R7 and R8. Resistors R7 and R8 maintain reverse biasing, and therefore a zener voltage of approximately 5.1V across diodes CR1 and CR2 respectively. If the input voltage at U2 pin 4 is excessively positive, CR120 will conduct, clamping the voltage at U2 pin 4 to + 5.7V (the zener voltage plus a diode drop). Similarly, if the input voltage at U2 pin 4 is excessively negative, CR119 and CR2 will clamp the voltage at − 5.7V. Resistor R6 has a 2 watt power rating to withstand high currents caused by improper voltages at the input.

High impedance buffering of the input and a signal gain of 25 dB is accomplished by the combination of dual

FET U2 (connected as a voltage follower), and amplifier U3. Divider R12 and R13 provides negative feedback for the circuit. High frequency compensation and stability are handled by C8. Dc balance corrections for this stage are made with R11.

Noninverting amplifier U4 has a selectable gain of 0, 10 or 20 dB determined by the output of U6 at pins 7, 8 and 14. For unity gain, U6 pin 7 is at + 15V, reverse biasing CR3, and U6 pins 8 and 14 are at − 15V, forward biasing CR4 and CR5. With CR3 reverse biased, no current flows through CR3 and R20, placing the drain and gate of Q3 at the same voltage. This turns Q3 on, shorting U4 pins 2 and 6 together. Since CR4 and CR5 are conducting, the gates of Q4 and Q5 are more negative than their drains, turning them off. A gain of 10 dB is achieved when U6 pin 8 is at + 15V and U6 pins 7 and 14 are at − 15V. CR4 is now reverse biased and CR3 and CR5 are forward biased. With CR4 reverse biased, no current flows through CR4 and R21, placing the drain and gate of Q4 at the same voltage. This turns Q4 on, shorting the junction of voltage divider R16 and R17 to U4 pin 2. These two resistors provide feedback (R16) and load resistance (R17) for amplifier U4. Since CR3 and CR5 are conducting, the gates of Q3 and Q5 are more negative than their drains, turning them off. A 20 dB gain is achieved when U6 pin 14 is at + 15V and U6 pins 7 and 8 are at − 15V. CR5 is reverse biased, turning on FET Q5 and shorting the junction of R18 and R19 to U4 pin 2. CR3 and CR4 are forward biased, turning off Q3 and Q4. R15 balances this stage. Table 5-21 shows the status of FETs Q3, Q4 and Q5 to obtain the proper gain for the selected full scale sensitivity.

Switchable attenuator R23 and R24 provides 5 dB of attenuation between U4 and U5. To activate the attenuator, U7 pin 1 goes to + 15V, reverse biasing CR6. This blocks current flow through R25, placing the drain and gate of Q6 at the same voltage. The bottom of R24 is shorted to ground through the source and drain of Q6. When U7 pin 1 goes to − 15V, CR6 is forward biased. Current flows through R25, turning off Q6 and disconnecting R24 from ground. Table 5-21 shows the status of FET Q6 to obtain the proper attenuation for the selected full scale sensitivity.

On the low pass filter channels, C15 and Q7 comprise an interstage coupling switch that eliminates accumulated dc voltages. If ac coupling has been programmed, Q7 is turned off and the signal is ac coupled through C15. When dc coupling is selected, Q7 effectively shorts C15 out of the circuit and dc couples the signal to U5. Q7 is deleted from Channel 1 on the Model 553A.

Amplifier U5 has a selectable gain of 0 or 20 dB determined by the output of U7 at pins 8 and 14. Control of this circuit is similar to the previously discussed U4 circuitry. For unity gain, U7 pin 8 is at + 15V and pin 14 is at − 15V. A gain of 20 dB is achieved when U7 pin 8 is at − 15V and pin 14 is at + 15V. R28 adjusts dc offset. Table 5-21 shows the status of FETs Q8 and Q9 to obtain the proper gain for the selected full scale sensitivity.

Signal gain and attenuation between TP1 and TP3 is controlled by quad operational amplifiers U6 and U7. All negative inputs to these amplifiers are held at approximately + 1.2V by CR112, CR113 and R260. The output polarity of each amplifier follows the respective positive input. For example, U6 pin 7 is at + 15V with pin 5 high, and − 15V with pin 5 low. These amplifiers are controlled by U8, an eight section D flip-flop. When LE1 goes high, the D inputs (labeled A through H from the amplifier/filter control circuitry) are transferred directly to their respective Q outputs, with pin 4 driving pin 5, pin 7 driving pin 6, and so on.

The signal at TP3 is attenuated 6.88 dB by voltage divider R262 and R263 to compensate for the filter stage (sheet 2) overall gain. The output signal at AMP 1, buffered by U94, is the input signal to the filter stage.

4.2.2 Overload Sense

Refer to schematic 0103-00-2364 sheet 2 of 5 for Model 552A, 0103-00-2872 for Model 553A. Except for component designators, the circuitry for channel 1 (shown on this sheet) and channel 2 (shown on sheet 3) is identical. Only channel 1 is discussed.

The input signal from the attenuator/amplifier circuit (AMP 1) enters quad comparator U10 at pins 7 and 8. Reference voltage divider R33 and R40 holds U10 pins 4 and 9 at about + 0.7V. Normally, U10 pin 8 is more negative than + 0.8V and pin 14 is saturated at + 15V. However, when an excessively positive voltage is present at AMP 1, the voltage at U10 pin 8 exceeds + 0.7V and pin 14 is forced to − 15V. This brings U10 pin 13 negative, turning on Q50 and bringing its emitter toward − 15V. Since the + input at U10 pin 5 is negative, pin 2 ($\overline{\text{OVLD 1}}$) goes low alerting the microprocessor of the overload on channel 1.

An excessively negative input voltage at AMP 1 is handled in a similar manner. Divider R37 and R39 holds U10 pin 6 at about − 0.7V. If the input voltage is excessively negative, U10 pin 1 will toggle from + 15 to − 15V as before. Again, U10 pins 13 and 5 go negative, bringing pin 2 ($\overline{\text{OVLD 1}}$) low. R41, C24 and Q50 act as a pulse stretcher to detect short duration pulses.

4.2.3 Filter

Although this discussion centers around operation of the low pass filter found in the Model 552A (both channels)

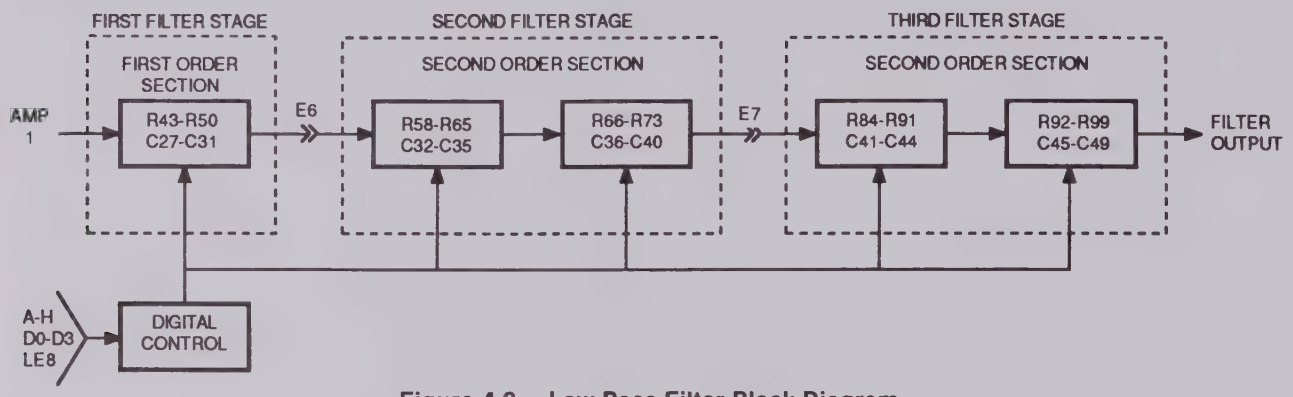


Figure 4-2. Low Pass Filter Block Diagram

and channel 2 of the 553A, it also applies to the high pass filter located in the Model 553A channel 1. Important differences between the two types of filters are noted, however, operation of the high pass filter is generally the reverse of the low pass filter. For example, the low pass filter characteristics are a mirror-image of the high pass filter characteristics. High pass filter circuitry is shown in schematic 0103-00-2872 sheet 2 of 5.

Refer to schematic 0103-00-2364 sheet 2 of 5, low pass filter block diagram figure 4-2 and filter stage characteristics, figure 4-3. Except for component designators, the circuitry for Model 552A channel 1 (shown on schematic sheet 2) and channel 2 (shown on schematic sheet 3) is identical. Only channel 1 is discussed. In addition, except for component values, the circuitry for Models 552A and 553A channel 2 (shown in schematic 0103-00-2872 sheet 3 of 5) are identical. All frequencies given in this discussion and filter characteristics shown in figure 4-3 are based on a programmed cutoff frequency of 2 kHz.

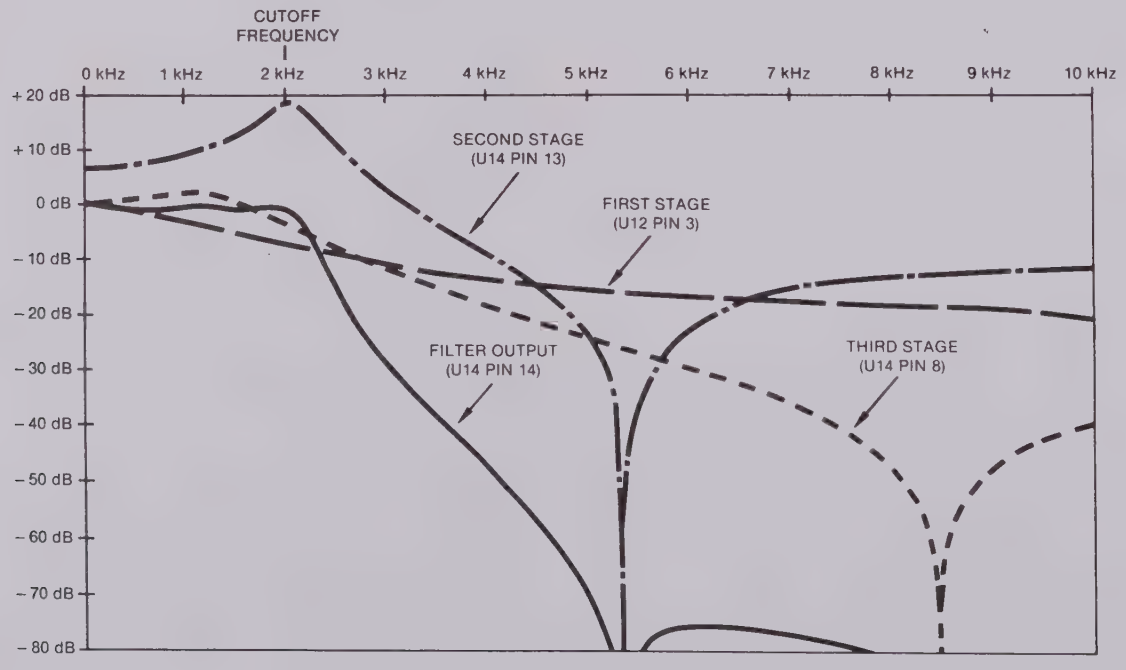


Figure 4-3. Filter Stage Characteristics

The three filter stages shown in figure 4-2 combine to produce a relatively flat response at and below the cutoff frequency (2 kHz), and a sharp drop in amplitude in the stopband (above 2 kHz).

Figure 4-3 shows the response characteristics of each stage, and the entire filter output. The second and third stage plots where obtained by connecting AMP 1 (from the attenuator/amplifier circuit) to the input of the respective stage. Note that at 0 kHz, the second stage plot begins at + 6.88 dB. This offsets the 6.88 dB of attenuation provided by R262 and R263 located in the attenuator/amplifier circuit. As shown, the first stage output gradually slopes negative as frequency increases. Below 1 kHz, the second and third stage amplitudes increase. The figure shows that the third stage peaks at ≈ 1 kHz while the second stage amplitude continues to increase until it peaks at ≈ 2 kHz. By proper placement of the second and third stage peaks, the combined effect of all three filters within the passband is a small amount of output ripple caused by the two peaks, but generally a flat output response.

From slightly above the cutoff frequency to less than 5 kHz, the approximate roll-off rate is 6 dB per octave for the first stage and 12 dB per octave for the second and third stages. Added together, they combine to provide a steep drop in filter output. Just above 5 kHz, the second stage output contains a sharp drop in amplitude or "zero" that pulls the filter output well below − 80 dB. "Zeros" will be explained later in this discussion. Between 5.5 kHz and 8 kHz, the filter output remains below − 72 dB because of the combined effect of all three filter stages. The third stage "zero" at 8.5 kHz again pulls the filter output below − 80 dB. Above 8.5 kHz, the three filter stages keep the filter output well attenuated.

Models 552A and 553A use "fifth order elliptic filters" consisting of one first order section, followed by two second order sections. The number of capacitors acting as energy storage elements in the filter section help determine the order. For example, a first order section has only one capacitor acting as an energy storage element, while a second order section has two. Each second order section contains low pass, high pass and bandpass outputs. A first order section low pass filter is simply a series resistor followed by a capacitor to ground. In the Model 552A, this stage can effectively be replaced with one resistor from E5 to U12 pin 3, and one capacitor from U12 pin 3 to ground. The signal is then buffered by U12.

In a second order section, the capacitors exchange energy most efficiently at the resonant frequency. The "Q" (quality) of a second order section is directly proportional to the efficiency (lack of energy loss) of this transfer. The higher the "Q", the higher the amplitude at the resonant frequency, peaking for "Q's" greater than 1. Figure 4-4 is a simplified schematic of the second filter stage. The "Q", and therefore peaking of the second stage is controlled by the feedback network R52, R55 and R56. The frequency location of this peak is determined by resistors R58 through R73 and capacitors C32 through C40.

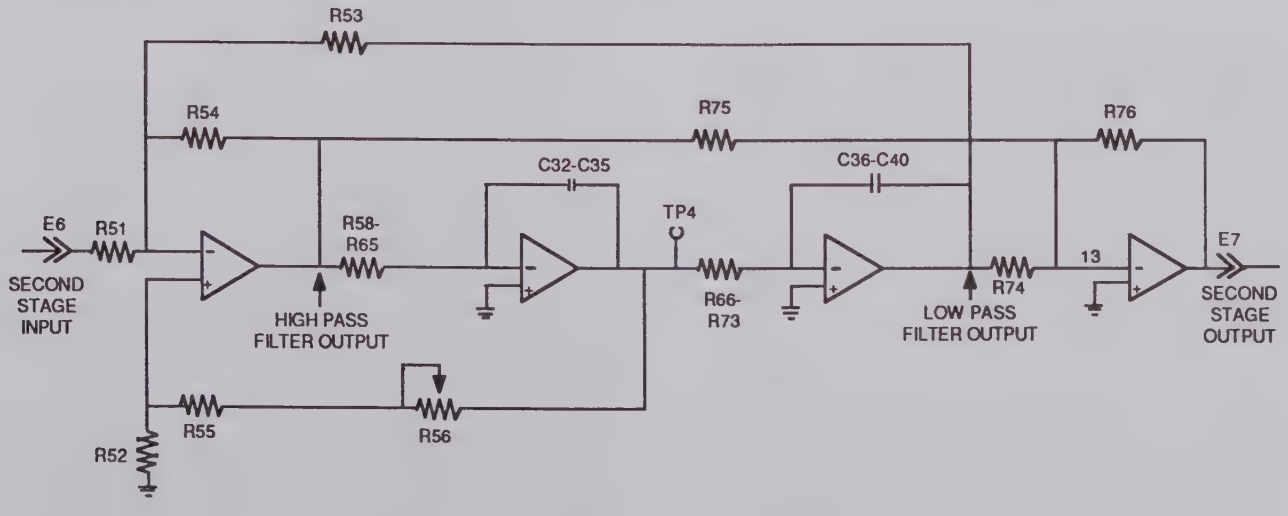


Figure 4-4. Second Filter Stage

A "zero" is a single frequency at which the output is sharply attenuated. The parallel connection of properly tuned low and high pass circuits contained within each second order section produces a transmission null or "zero" at a frequency determined by the output amplitude, frequency and phase relationships of the two circuits. Since a proper match of these low pass and high pass circuits shift phase in equal but opposite directions, the sum produced by the parallel connection serves actually to produce the difference between these amplitudes. When the signals are equal in amplitude the output voltage is zero.

In the second filter stage, the amplitude, and phase relationship of these filters, is determined by the relative value of fixed resistors R74 (low pass output) and R75 (high pass output). The ratio between R74 and R75 determines the frequency of the "zero". In the low pass filter contained in the Model 552A and channel 2 of the Model 553A, frequencies above the "zero" need greater attenuation then frequencies below the "zero". Therefore, R75 is larger than R74. In the high pass filter of Model 553A channel 1, attenuation conditions, and therefore the value of R74 and R75 are reversed.

Fixed value components within the second order sections determine the shape of each plot, while the selectable components set the peak and therefore the zero frequency locations with two digits of resolution.

The selectable resistors are switched in or out of the circuit by FETs Q10 through Q49 (see table 5-28), driven by op amps U21 and U22 through diodes CR10 through CR49. When Q10 is selected to connect R43, U21 pin 1 goes to +15V. This reverse biases CR10, preventing current from flowing through CR10 and the connected 47 KΩ resistor located in resistor pack U11. This places the drain and gate of Q10 at the same voltage, turning the FET on and connecting E5 to R43. If R43 is to be disconnected, U21 pin 1 goes to −15V, forward biasing CR10. With CR10 forward biased, current flows through CR10 and the connected 47 KΩ resistor located in resistor pack U11. This places the gate more negative than the drain, turning the FET off and disconnecting E5 from R43. The remaining resistors are switched in or out of the circuit in the same manner.

U21 and U22 are quad operational amplifiers with all negative inputs held at approximately +1.2V by CR50, CR51 and R111. The output polarity of each amplifier follows the respective positive input. For example, if U21 pin 5 is high, pin 7 will be +15. However, if U21 pin 5 is low, pin 7 will be −15. These amplifiers are controlled by U23, an eight section D flip-flop. When LE2 goes high, the D inputs (labeled A through H from the amplifier/filter control circuitry) are transferred directly to their respective Q outputs, with pin 3 driving pin 2, pin 4 driving pin 5, and so on.

Enabling and disabling of capacitors C27 through C49 is handled by relays K5 through K13 (see table 5-27) driven by inverting driver U20. "D" flip-flop U24 is driven directly from the digital microprocessor section. When LE6 goes high, the D inputs (labeled D0 through D3) are transferred directly to their respective Q outputs, with pin 4 driving pin 2, pin 5 driving pin 7, and so on. U28 is a 1K ohm resistor bank used to pull up the output lines from U24.

The output at J6 can be the same amplitude as the filter or amplified +10 dB. Amplifier U19 has a gain of 10 dB, however if switchable 10 dB attenuator, R105 driven by K14 and U20 is activated, the amplitude at J6 will be the same as the output of the filter. K14 is controlled from the front panel with the Output Gain button.

4.2.4 Digital Control Circuitry

Refer to figure 4-5 and schematic 0103-00-2364 sheet 4 of 5. The Z80 microprocessor section is the heart of all the digital control circuitry for the instrument. The major components are the Z80 microprocessor (U53), EPROM (U60), RAM (U57) and address decoder (U58).

The instrument uses clock signals of 102.4 kHz (100 kHz), 1.024 MHz (1 MHz) and 2.048 MHz (2 MHz) originating from the 10.24 MHz oscillator U51 and divider U52. At initial power up, the clock oscillator is unstable for several cycles, causing the internal state and I/O ports to be random. To prevent transferring erroneous data during this time, the microprocessor is disabled by holding U53 pin 26 low when the unit is first turned on. This condition remains in effect for a minimum of 20 ms as C125 charges to a predetermined level.

The Z80 accepts commands from the keyboard and remote interfaces. It issues commands to the remote interfaces, display, and analog signal conditioning circuits for both channels. To increase the load capability of the microprocessor, these commands are handled through buffers U54, U55 and bidirectional buffer U56. Software programs stored in EPROM U60 dictate instrument routines run by the microprocessor. The EPROM is addressed by the "A" bus (A0-A14) when chip enable ($\overline{CE}$) at pin 20 is pulled low.

As operating parameters are updated, they are sent to the instrument control circuits and front panel display via data lines D0 through D7. These parameters are also stored in, then later retrieved from, the scratch pad memory, U57, when chip select ($\overline{CS}$) at pin 18 is brought low. Address lines A0 through A10 determine the location of the stored information that travels on bi-directional

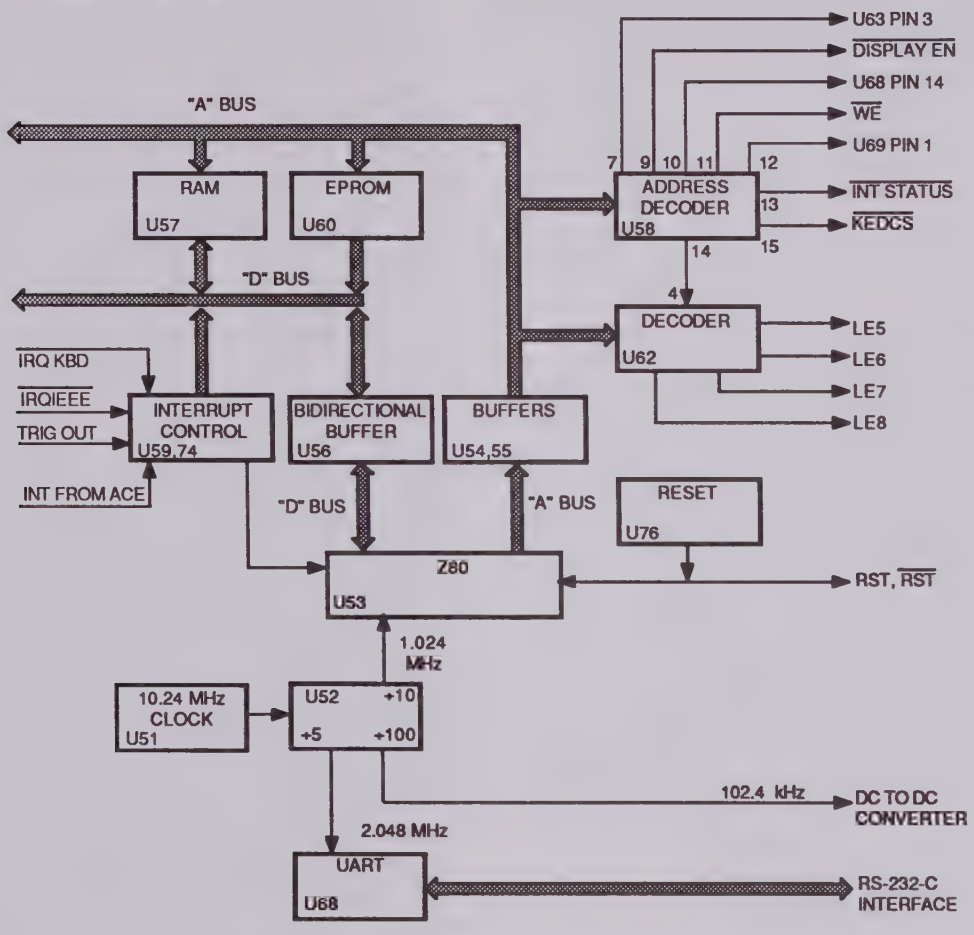


Figure 4-5. Digital Control Block Diagram

data lines D0 through D7. To write data into RAM, the output is disabled by a high on pin 20 ($\overline{OE}$) and a low on pin 21 ($\overline{WE}$). Reading data from RAM is accomplished by leaving $\overline{WE}$ high and bringing $\overline{OE}$ low.

The clearinghouse for most operations is the address decoder, U58. It decodes address lines A10 through A15, then pulls the appropriate output line low (true). These lines control the GPIB bus (pin 7), front panel board display (pin 9), RS-232-C bus (pin 10), opto driver U86 located on sheet 5 (pin 11), RS-232-C baud rate switch buffer U69 (pin 12), interrupt status buffer U59 (pin 13) and front panel keyboard encoder U1 (pin 15). If both $\overline{RD}$ and $\overline{WR}$ are high, U63 pin 3 ($\overline{CS}$) will also be high. When selected by U58 pin 14, U62 decodes A7, A8 and A9 to enable control lines LE5 through LE8.

Any of four events will interrupt the Z80 microprocessor. These are; 1) a keyboard button being pressed (IRQ KBD) unless 'L0' (local lockout) has been remotely issued; 2) data arriving from the IEEE bus ($\overline{IRQIEEE}$); 3) a GET command originating from the IEEE bus (TRIG OUT from U63 pin 24) and; 4) data arriving from the RS-232-C interface (INT FROM ACE). These interrupts enter U75 pins 1, 2, 4 and 5 where they are logically OR'd before reaching the Z80 at pin 16. If any interrupt is enabled, the microprocessor will read the interrupt status from U59 at pins 3, 5, 7 and 9 to locate the interrupt source.

If the front panel has not been disabled remotely and a key is pressed, J1 pin 22 (IRQKBD) will go high, bringing U75 pin 1 low. This causes an interrupt at U53 pin 16. The microprocessor will then check the "D" bus lines to locate the interrupt source. Because IRQKBD (U59 pin 17) is high, U59 pin 3 will pull D3 high, designating a keyboard interrupt. After reading the front panel keyboard, IRQKBD returns low, disabling the interrupt. When data arrives on the IEEE bus, U63 pin 40 pulls $\overline{IRQIEEE}$ and U75 pin 5 low, initiating the interrupt

sequence. After the microprocessor reads the IEEE input, the $\overline{IRQIEEE}$ line is returned high. If the IEEE bus receives a GET (Group Execute Trigger), U63 pin 24 pulls TRIG OUT high. The interrupt sequence is initiated because U75 pin 2 is now low. Data or an error originating from the RS-232-C interface is detected by U68. Pin 30 (INT FROM ACE) is forced high, initiating the interrupt sequence.

Opto-isolators U70 and U71 signal the microprocessor section (through U59) of a filter overload.

4.2.5 Amplifier/Filter Control

Refer to schematic 0103-00-2364 sheet 5 of 5 for Model 552A, 0103-00-2872 for Model 553A. The amplifier/filter control section directs programming information to the appropriate circuit. With each pulse at D2 (SHIFT CLK), data and address information is clocked from D1 (DATA OUT) through register U86 and opto-isolator U88 into address register U91 and data register U92. After the programming information has settled, only one of the U91 output lines (pins 3, 4, 5 or 6) will be high. This determines the destination (LE1, LE2, LE3 or LE4) of the eight bit data word ("A" through "H") in U92. A load enable pulse at D0 (MLE) passes through opto-isolator U87 to bring U93 pin 10 high, enabling the appropriate control line, LE1 through LE4. U87, U88 and U89 provide isolation between the digital control and analog sections of the instrument.

4.2.6 IEEE-488 Remote Interface

Refer to schematic 0103-00-2364 sheet 4 of 5 for Model 552A, 0103-00-2872 for Model 553A. For the IEEE-488 interface, most of the protocol functions are handled by the General Purpose Interface Adapter (GPIA). This is a single IC (U63) that meets all the handshaking requirements of the 1978 IEEE-488 standard. Data and control portions of the bus require high current driving capability and specific line termination provided by bus drivers, U64 and U65. When there is a pending interrupt, $\overline{IRQ}$ (U63 pin 40) is asserted low. This alerts the microprocessor of an interrupt condition, causing it to interrogate the eight registers internal to U63. Data from the IEEE-488 bus (listen mode) is accessed by reading from the data registers in U63; data output (talk mode) is written to the same register location.

The DIP address switch, S1, selects the GPIB address for the instrument. Pull-up resistors (U84) hold input lines to U82 high unless S1 pulls one or more of these lines low. A low at the address strobe enable line ($\overline{ASE}$) from U63 enables the output of U82, and therefore, S1. The microprocessor reads the switch by reading data lines D0 through D7 from U82.

4.2.7 RS-232-C Remote Interface

Refer to schematic 0103-00-2364 sheet 4 of 5 for Model 552A, 0103-00-2872 for Model 553A. When selected by a low at U58 pin 10, UART U68 encodes characters for transmission in RS-232-C standard format. A generator within the UART produces baud rates of 110 to 9600 as programmed by software and derived from the 2MHz clock input at pin 16. Data is transferred to and from the internal bus lines D0-D7 and A0-A2 as determined by the status of control lines $\overline{RD}$ and $\overline{WR}$. Receiver U67 accepts inputs from the RS-232-C interface, inverting and forwarding them to U68. Driver U66, powered by the ±12V supply (see schematic 0103-00-2364 sheet 5), inverts and buffers the UART output to drive the RS-232-C interface.

4.2.8 ± 12V DC Supply

Refer to schematic 0103-00-2364 sheet 5 of 5 for Model 552A, 0103-00-2872 for Model 553A. The ± 12V dc supply is a +5 to ±12V dc to dc converter. It provides the proper voltages required by U66 to drive the RS-232-C interface. Current drain from this supply is very low (± 25ma). The 100 kHz signal from U52 pin 13 in the Z80 circuit drives the base of Q101 and Q102. The collectors of these transistors drive the base of Q103 such that this transistor is forced hard on and hard off, creating a peak to peak swing of about 25V at the collector. CR116 half-wave rectifies this voltage for the +12V supply, while voltage doubler C160, CR117 and CR118 increase the negative voltage swing to −12V at the output terminal. Electrolytic capacitors C159 and C161 provide filtering, and resistors R270 and R271 provide needed loading for the +12V and -12V supplies respectively.

4.3 FRONT PANEL BOARD

Refer to figure 4-6 and schematic 0103-00-2365 sheet 1 of 1. The front panel board assembly contains the keyboard, status LEDs, and two LCD displays. The keyboard provides manual control of the instrument unless it has been overridden by a remote command. Front panel LEDs indicate the status of various remote functions. The liquid crystal displays indicate the programmed attenuation or amplification of the input signal and cutoff frequency of each filter channel.

Keyboard controller U1 directs the operation of both the front panel keyboard and LEDs. The keyboard is an XY matrix of switches. U1 pins 32 through 34 (S0 through S2) continuously clock a binary count of 0 through 7 to U7 pins 1, 2 and 3. At one end of the switch matrix, the decoded output of U7, (Y0 through Y2) sequentially strobes each line low. At the other end of the matrix, the R0 through R7 (U1 pins 1, 2, 5 through 8, 38 and 39)

lines are all held high by internal pull-up resistors. When a key is pressed and the line for that key is strobed low, the corresponding line (one of R0 through R7) goes low, the interrupt request line (IRQ) at pin 4 is brought high, and the Z80 microprocessor on the mainboard interrogates DB0 through DB7 (U1 pins 12 through 19). After determining which key was pressed, the IRQ line is again brought low.

If either the RS-232-C interface or IEEE-488 bus issues a front panel disable command, the microprocessor will bring U7 pin 4 high (through U4 pin 19). When this occurs, the U7 output pins (Y0 through Y2) remain high, disabling the front panel keys.

For any front panel LED to be lit, the cathode line (U2 pin 3) must be low, and the appropriate U3 output line (pins 11 through 18) must be high. As mentioned in the keyboard description, S0 through S2 continuously clock a binary count of 0 through 7. The 8 bit for this count, provided by S3, increases the count to 16. This bit, which drives U2 pin 1, has a 50% duty cycle, toggling at 0 and 8.

A small memory within U1 drives the eight ports (U1 pins 24 through 31) that control power driver U3. These amplifiers drive the appropriate output pin of U3 high. Suppose the "TALK" LED is to be lit. S3 will be high, making U2 pin 3 and the "TALK" LED cathode low. U1 pin 27 will be high only for the 8 cycles that S3 is high, forcing U3 pin 14 and the anode of the "TALK" LED high. This lights the LED, but at the 50% rate described above. When U2 pin 3 returns high, the LED is extinguished. Due to the modulation rate, the LED appears to always be lit.

Flip-flop U4 buffers serial information between the Z80 microprocessor (data line D0) and pin 9 (S_I) of the display driver U5. Liquid crystal displays (LCD) DS1 and DS2 receive this information when U5 pin 10 (CS) is high and pin 8 (SCK) is clocked by data line D1 (through U4). This information is either a command (U5 pin 12 high) or data (U5 pin 12 low).

U5 pins 15, 16, 17 and 19 through 51 control specific LCD segments. U5 continually strobes and updates the display information according to the input at pin 9. The LCD is set for optimum viewing at the factory with trim pot R12.

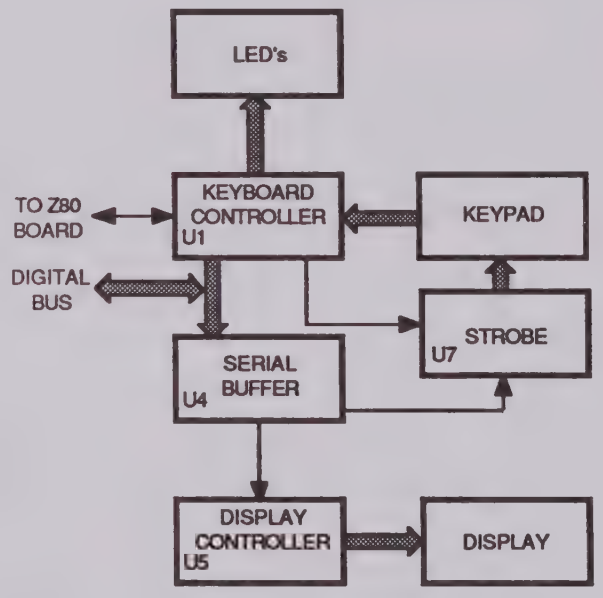


Figure 4-6. Front Panel Block Diagram

SECTION 5
MAINTENANCE

5.1 INTRODUCTION

The maintenance section contains the conformance, calibration and troubleshooting procedures. Before starting either the conformance or calibration procedures, errors caused by the external attenuator used in these procedures must be cataloged. Refer to paragraph 5.2 to log this data.

The conformance procedure located in paragraph 5.3 should be used to verify instrument performance at least once a year. If any step within the conformance procedure does not meet specification, do a complete calibration of the failed channel (paragraph 5.4). If the instrument cannot be calibrated, refer to the troubleshooting procedure, paragraph 5.5. If the analog portion of either channel is repaired, a complete calibration of that channel is required.

5.2 EXTERNAL ATTENUATOR ERROR LOGGING

Errors caused by the external attenuator used in the conformance and calibration procedures may give erroneous readings and must be cataloged.

5.2.1 Required Test Equipment

Table 5-1 lists the test equipment required to log the external attenuator errors.

Table 5-1. Required Test Equipment

Equipment	Quantity	Specifications	Suggested Equipment
DVM	1	True RMS 4½ digit resolution	Fluke Model 8050A
Signal Source	2	100 Hz to 50 kHz sine wave at 1 mV to 1 Vrms	Wavetek Model 5100
Attenuator	1	0 to 60 dB of attenuation in 5 dB steps ± 0.01 dB Accuracy 50 Ω Input	Kay Model 30-0 432C

5.2.2 Error Logging Procedure

Only the six left switches on the attenuator (designated 20-20-20-20-10-5) are used. The three right switches remain OFF. For example, an attenuator setting shown in this procedure as "20-0-0-0-0-5" means that only the left most and fifth from right switches are ON, all others are OFF.

To determine attenuator errors, perform the following steps.

1. Make copies of tables 5-2, 5-3 and "Input Gain Accuracy" (table 5-6).
2. Set signal source to 100 Hz, 10 Vp-p.
3. Set DVM range to 200 mV, ac, Mode to dB.
4. Connect attenuator between signal source and DVM.
5. Set attenuator to 20-0-0-0-0-0.
6. Push DVM RELATIVE button in to zero readout.
7. Set attenuator to 20-20-0-0-0-0.
8. Record the DVM reading (to 0.01 dB) in table 5-2 column "A" but do not enter plus or the minus signs.
9. Subtract the number in column "B" (20) from the number in column "A" and enter the result, with plus or minus signs, in column "C".

Example 1: DVM reading = −20.04
Column A entry = 20.04 (note minus sign is deleted)
Column C entry = 20.04 − 20 = +0.04

Example 2: DVM reading = −19.92
Column A entry = 19.92 (note minus sign is deleted)
Column C entry = 19.92 − 20 = −0.08

10. Repeat steps 8 and 9 for the remaining attenuator settings listed in table 5-2.
11. Copy the results from table 5-2 column "C" (steps 1 through 5) to the appropriate location in the correction factors column in table 5-3. For example, for the row labeled "35" (dB of attenuation required) in table 5-3, enter the values recorded in column "C" steps 4 and 5, including plus and minus signs. Note that some required attenuation settings, such as "25", only have one correction factor and are entered directly into the "Total Correction" column.
12. Add the correction factors for each required attenuation, noting plus and minus signs for each factor. Enter the sum in the "Total Correction" column.
13. Transfer the "Total Correction" column values (with signs) from table 5-3 into the Correction Factor column in the Input Gain Accuracy test, table 5-6.

Table 5-2. Individual Attenuator Switch Errors (Reproducible)

Step	Attenuator Switch Setting	Column A	Column B	Column C (Column A-Column B)
1	20-20-0-0-0-0		20	
2	20-0-20-0-0-0		20	
3	20-0-0-20-0-0		20	
4	20-0-0-0-10-0		10	
5	20-0-0-0-0-5		5	

Table 5-3. Total Attenuation Errors (Reproducible)

Required Attenuation	Attenuator Setting	Correction Factors From Table 1 Column C	Total Correction
20	20-0-0-0-0-0	No Correction Needed	0 dB
25	20-0-0-0-0-5	(Step 5 Only)	_____ dB
30	20-0-0-0-10-0	(Step 4 Only)	_____ dB
35	20-0-0-0-10-5	_____ (Step 4) + _____ (Step 5) =	_____ dB
40	20-20-0-0-0-0	(Step 1 Only)	_____ dB

Table 5-3. Total Attenuation Errors (Reproducible) (Cont)

Required Attenuation	Attenuator Setting	Correction Factors From Table 1 Column C	Total Correction
45	20-20-0-0-0-5	_____ (Step 1) + _____ (Step 5) =	_____ dB
50	20-20-0-0-10-0	_____ (Step 1) + _____ (Step 4) =	_____ dB
55	20-20-0-0-10-5	_____ (Step 1) + _____ (Step 4) + _____ (Step 5) =	_____ dB
60	20-20-20-0-0-0	_____ (Step 1) + _____ (Step 2) =	_____ dB
65	20-20-20-0-0-5	_____ (Step 1) + _____ (Step 2) + _____ (Step 5) =	_____ dB
70	20-20-20-0-10-0	_____ (Step 1) + _____ (Step 2) + _____ (Step 4) =	_____ dB
75	20-20-20-0-10-5	_____ (Step 1) + _____ (Step 2) + _____ (Step 4) + _____ (Step 5) =	_____ dB
80	20-20-20-20-0-0	_____ (Step 1) + _____ (Step 2) + _____ (Step 3) =	_____ dB

5.3 CONFORMANCE TEST PROCEDURE

The conformance test procedure, used to verify that the instrument is within specification, should be performed at least once a year. Before starting this test, list data errors (paragraph 5.2) caused by the external attenuator.

If any step within this test does not meet specification, do a complete calibration of the failed channel (paragraph 5.4).

5.3.1 Required Test Equipment

Table 5-4 lists the test equipment required to perform the conformance procedure located in table 5-5.

Table 5-4. Required Test Equipment

Equipment	Quantity	Specifications	Suggested Equipment
DVM	1	True RMS 4½ digit resolution	Fluke Model 8050A
Spectrum Analyzer	1	To 50 kHz	Hewlett Packard Model 3580A
Phase Meter	1	1 MHz Bandwidth 0.05° Accuracy 0.01° Resolution	Dranetz Chassis: Model 305C/102,107 MOD 14 Module: 305-PA-3009

Table 5-4. Required Test Equipment (Cont)

Equipment	Quantity	Specifications	Suggested Equipment
Signal Source	2	100 Hz to 50 kHz sine wave at 1 mV to 1 Vrms	Wavetek Model 5100
Attenuator	1	0 to 60 dB of attenuation in 5 dB steps ± 0.01dB Accuracy 50 Ω Input	Kay Model 30-0 432C
Low Noise Signal Source	1	All harmonic components – 80dB below fundamental	Hewlett Packard Model 239
50Ω Termination	1	Feedthrough, 0.1% accuracy, 2W	
Coaxial Cables	4	BNC male connectors, RG-58U cable	
BNC Tee	1	1 male to 2 female connection	
Resistor	2	1kΩ, 1/4W	

Spectrum Analyzer Initial Settings:

DISPLAY	CLEAR WRITE
POWER	ON
ADAPTIVE SWEEP	OFF
AMPLITUDE MODE	1 dB/Div (LOG)
AMPLITUDE REFERENCE LEVEL	NORMAL, dBV/LIN
INPUT SENSITIVITY	0 dBV
INPUT SENSITIVITY VERNIER	Fully cw (CAL)
START/CTR	START
FREQUENCY FINE (Vernier)	000
RESOLUTION BAND-WIDTH	10 Hz
DISPLAY SMOOTHING	MIN
FREQ SPAN/DIV	50 Hz
SWEEP TIME/DIV	1 sec
SWEEP MODE	LOG

Model 552A/553A Initial Settings:

Channel Select	Both channels
FULL SCALE	0dBV
CUTOFF FREQ	10X1kHz
Output Gain	0
AC/DC Coupling	DC
Digital Common (Rear Panel)	Earth/Chassis
Analog Common (Rear Panel)	Earth/Chassis

Connect the instrument to the ac power source and allow it to warm up at least 30 minutes before testing.

NOTE

Subheadings used in table 5-6, Conformance Test Report, are keyed to test names listed in the Check column of table 5-5. Before starting, copy table 5-6, then use this copy to record the results of each Conformance Procedure test.

Table 5-5. Conformance Procedure

Step	Check	Tester	Tester Setting	Instrument Setting	Specification	Remarks
1	DC Offset	DVM	DC, 200 mV	See paragraph 5.3.1	±10 mV	Short Input 1 to ground. With front panel DC Adj, set Output 1 to 0 ± 0.5 mV. Record dc offset for each Channel 1 FULL SCALE setting shown.
2				FULL SCALE: 0 dBV		Move short from Input 1 to Input 2. With front panel DC Adj, set Output 2 to 0 ± 0.5 mV. Record dc offset for each Channel 2 FULL SCALE setting shown.
3	Input Gain Accuracy	DVM	AC (dB), REF: 1000 Ω	AC coupling, FULL SCALE: 0 dBV	Zero meter reading	Remove short from Input 2. Inject 1 kHz 10 Vp-p sine wave (at source) through attenuator to DVM. Push RELATIVE button on DVM in to zero meter reading.
		Attenuator	20-0-0-0-0-0			
		Signal Source	See Remarks column			
4			See Attenuator Setting column in Input Gain Accuracy chart (table 5-6)	See FULL SCALE Setting column in Input Gain Accuracy chart (table 5-6)	0 ±0.1 dB for amplitude match at dc Other settings are ±0.2 dB	Move cable from DVM input to Model 552A/553A Input 1 and connect Output 1 to DVM input. Record Measurements for each Channel 1 setting, then add the Correction Factor values to obtain the correct Result.
5						Move cables from Model 552A/553A Input 1 to Input 2 and from Output 1 to Output 2. Record Measurement for each Channel 2 setting listed, then add the Correction Factor values to obtain the correct Result.

Table 5-5. Conformance Procedure (Continued)

Step	Check	Tester	Tester Setting	Instrument Setting	Specification	Remarks
6	Output Gain Accuracy	DVM, Signal Source		FULL SCALE: 0 dBV	Zero meter reading	Move cable from Model 552A/553A Input 2 to Input 1 and from Output 2 to Output 1. Push RELATIVE button on DVM twice to zero meter reading.
		Attenuator	20-0-0-0-0-0			
7				10 dB Output Gain On	±0.2 dB	Record meter reading.
8				10 dB Output Gain Off	Zero meter reading	Move cable from Model 552A/553A Input 1 to Input 2 and from Output 1 to Output 2. Push RELATIVE button on DVM twice to zero meter reading.
9				10 dB Output Gain On	±0.2 dB	Record meter reading.
10	Cutoff Frequency Accuracy	DVM, Signal Source	(DVM) AC, Range: 2V, RELATIVE: Off	10 dB Output Gain Off	0 ±0.5 dBV	Inject 1 kHz sine wave into DVM and adjust signal source amplitude.
11				CUTOFF FREQ: See chart (table 5-6)	Low pass filter: 0 to +3% at −0.5 dB point (above pass-band) High pass filter: 0 to −3% at −0.5 dB point (below pass-band)	Move injected signal from DVM to Input 1 and connect Output 1 to DVM input. Do the following six steps for each Channel 1 CUTOFF FREQ Setting. Move cable from Model 552A/553A Input 1 to Input 2 and from Output 1 to Output 2. Do the following six steps for each Channel 2 CUTOFF FREQ Setting.

1) Set the instrument to the CUTOFF FREQ shown in chart.
2) (Skip this step when doing the high pass filter above a CUTOFF FREQ of 20 kHz.) Set the injected signal frequency as follows:
   Low pass filter; one-tenth the CUTOFF FREQ.
   High pass filter; ten times the CUTOFF FREQ.
3) (Skip this step when doing the high pass filter above a CUTOFF FREQ of 20 kHz.) Push DVM RELATIVE button "out" then "in" to zero reading (0.00 dB).
4) Set signal source output frequency to the CUTOFF FREQ.
5) Adjust signal source frequency for a reading of −0.50 dB.
6) Record signal source output frequency reading on chart.

Table 5-5. Conformance Procedure (Continued)

Remove cables connected to the instrument Input 2 and Output 2 connectors. Jumper a coaxial cable from the spectrum analyzer rear panel TRACKING OSCILLATOR OUT connector to the instrument Input 1 connector. Connect Output 1 on the instrument to the spectrum analyzer input. Adjust the LEVEL control (on the analyzer rear panel) for a display of −1dBV.

Step	Check	Tester	Tester Setting	Instrument Setting	Specification	Remarks
12	Passband Flatness (Models 552A and 553A) and Amplitude Matching (Model 552A only)	Spectrum Analyzer	See paragraph 5.3.1	See CUTOFF FREQ Setting column in Passband Flatness chart (table 5-6)	Flatness: 0.5 dB p-p ripple Matching (Model 552A only): ±0.1dB for frequencies of dc to 0.8 f_c ±0.2 dB for frequencies of >0.8 f_c to f_c	Do the following eight steps.

1) Set the instrument CUTOFF FREQ and spectrum analyzer controls as shown in the chart (table 5-6).
2) Record the maximum passband ripple (flatness). Press STORE (Model 552A only).
3) Move cables from Model 552A/553A Input 1 to Input 2 and from Output 1 to Output 2.
4) Record the Channel 2 maximum passband ripple.
5) For the Model 552A, record the maximum passband amplitude difference (matching) between channel 1 and channel 2 for the frequencies shown. (Delete for Model 553A.)
6) Deselect STORE (Model 552A only).
7) Move cables from Model 552A/553A Input 2 to Input 1 and from Output 2 to Output 1.
8) Repeat steps 1 through 8 for each remaining CUTOFF FREQ in the chart (table 5-6).

13	Stop Band Attenuation		FREQUENCY SPAN/DIV: 500 Hz for low pass filter; 200 Hz for high pass filter. RESOLUTION BANDWIDTH: 100 Hz for low pass filter, 30 Hz for high pass filter.	CUTOFF FREQ: 1 kHz	All signals below −72 dB (−75 dBV)	Deselect STORE. Connect Output 1 to spectrum analyzer INPUT. Inject 1 kHz sine wave at Input 1. Adjust sine wave amplitude (1 kHz component) for 0 dBV at analyzer.
14			INPUT SENSITIVITY −70 dBV			Change signal source frequency to 2.56 kHz for low pass filter, 390 Hz for high pass filter. Record level of 2.56 kHz (390 Hz for high pass filter) component on analyzer.
15			INPUT SENSITIVITY: 0 dBV			Move cables from Input 1 to Input 2 an from Output 1 to Output 2. Change signal source frequency to 1 kHz. Adjust sine wave amplitude (1 kHz component) for 0 dBV at analyzer.

Table 5-5. Conformance Procedure (Continued)

Step	Check	Tester	Tester Setting	Instrument Setting	Specification	Remarks
16	Stop Band Attenuation (Cont)	Spectrum Analyzer	INPUT SENSITIVITY: −70 dBV	CUTOFF FREQ: 1 kHz	All signals below −72 dB (−75 dBV)	Change signal source frequency to 2.56 kHz for low pass filter, 390 Hz for high pass filter. Record level of 2.56 kHz (390 Hz for high pass filter) component on analyzer.
17			FREQUENCY SPAN/ DIV: 5 kHz for low pass filter; 2 kHz for high pass filter, RESOLUTION BAND-WIDTH: 300 Hz, INPUT SENSITIVITY: 0 dBV	CUTOFF FREQ: 10 kHz		Change signal source frequency to 10 kHz. Move cables from Input 2 to Input 1 and from Output 2 to Output 1. Adjust sine wave amplitude (10 kHz component) for 0 dBV at analyzer.
18			INPUT SENSITIVITY: −70 dBV			Change signal source frequency to 25.6 kHz for low pass filter, 3.9 kHz for high pass filter. Record level of 25.6 kHz (3.9 kHz for high pass filter) component on analyzer.
19			INPUT SENSITIVITY: 0 dBV			Move cables from Input 1 to Input 2 and from Output 1 to Output 2. Change signal source frequency to 10 kHz. Adjust sine wave amplitude (10 kHz component) for 0 dBV at analyzer.
20			INPUT SENSITIVITY: −70 dBV			Change signal source frequency to 25.6 kHz for low pass filter, 3.9 kHz for high pass filter. Record level of 25.6 kHz (3.9 kHz for high pass filter) component on analyzer.

Table 5-5. Conformance Procedure (Continued)

Step	Check	Tester	Tester Setting	Instrument Setting	Specification	Remarks
21	Harmonic Distortion	Low Noise Signal Source	Frequency: 2 kHz, Amplitude: 0dBV	CUTOFF FREQ: 50 kHz for low pass filter; 100 Hz for high pass filter.	All signals below −72 dB (−75 dBV)	Connect Low Noise Signal Source output to Model 552A/553A Input 1 Connect Output 1 to Spectrum Analyzer INPUT. Record highest harmonic level (at multiples of 2 kHz). Move cables from Input 1 to Input 2 and from Output 1 to Output 2. Record highest harmonic level (at multiples of 2 kHz).
		Spectrum Analyzer	FREQUENCY SPAN/DIV: 1 kHz, RESOLUTION BANDWIDTH: 100 Hz, INPUT SENSITIVITY: 0 dBV, AMPLITUDE MODE: 1 dB/DIV			
22	Intermodulation Distortion (Model 552A only. For Model 553A, go to step 25.)	Standard Signal Source	Frequency 2 kHz	CUTOFF FREQ: 20 kHz		Connect as shown in figure 5-3 (Output 1) and adjust both signal source amplitudes for displays of −6 dBV.
		Low Distortion Signal Source	Frequency 3 kHz			
		Spectrum Analyzer				
23		Spectrum Analyzer	INPUT SENSITIVITY: −70 dBV			Change standard signal source frequency from 2 kHz to 35 kHz. Change low distortion signal source frequency from 3 kHz to 40 kHz. Record level of 5 kHz component.
24						Move cable from Output 1 to Output 2. Record level of 5 kHz component. Disconnect signal at Input 1 and Input 2.

Table 5-5. Conformance Procedure (Continued)

Step	Check	Tester	Tester Setting	Instrument Setting	Specification	Remarks
25	Line Related Spurs	Spectrum Analyzer	FREQUENCY SPAN/ DIV: 20 Hz, RESOLUTION BANDWIDTH: 10 Hz, SWEEP RATE: .5 S/DIV, AMPLITUDE MODE: 10 dB/DIV, INPUT SENSITIVITY: − 60 dBV	CUTOFF FREQ: Low pass filter; 20 kHz. High pass filter; 100 Hz. See FULL SCALE Setting column in Line Related Spurs chart (table 5-6)	− 72 dB below full scale for input sensitivity ⩾ − 50 dBV − 65 dB below full scale for input sensitivity of − 55 dBV. − 60 dB below full scale for input sensitivity of − 60 dBV	Short Input 1 to ground. Connect Output 1 to analyzer INPUT. Record worst case line component level (at multiples of 60 Hz) for each FULL SCALE setting shown. Move short from Input 1 to Input 2 and cable from Output 1 to Output 2. Record worst case line component level (at multiples of 60 Hz) for each FULL SCALE setting shown.
26	Phase Matching (Model 552A only)	Phase Meter	Calibration Mode: MEAS, Display: Φ Angle, Bandwidth: >12 Hz	See CUTOFF FREQ Setting column in Phase Matching chart (Table 5-6)	± 1° from dc to 0.8 f_c ± 2° from >0.8 f_c to f_c	Connect signal source output to Input 1 and Input 2. Connect Output 1 to REFERENCE input and Output 2 to signal input of phase meter. Record phase difference for each setting shown.
		Standard Signal Source	Frequency: 80Hz, Amplitude: 0 dBV			
27	Noise Floor	DVM		CUTOFF FREQ: 50 kHz for low pass filter; 100 Hz for high pass filter, FULL SCALE: + 20 dBV	At + 20 dBV FULL SCALE sensitivity: Low pass filter; ⩽1.0 mVrms. High pass filter; <6.0 mVrms. At − 60 dBV FULL SCALE sensitivity: Low pass filter; 10 mVrms. High pass filter; 30 mVrms.	Short Input 1 to ground. Connect Output 1 to voltmeter input. Record result for each FULL SCALE setting shown (table 5-6). Move short from Input 1 to Input 2 and cable from Output 1 to Output 2. Record result for each FULL SCALE setting shown.

Table 5-6. Conformance Test Report (Reproducible)

DC Offset

Channel 1		Channel 2	
FULL SCALE Setting	Result	FULL SCALE Setting	Result
+ 20 dB	_____	+ 20 dB	_____
+ 10 dB	_____	+ 10 dB	_____
+ 5 dB	_____	+ 5 dB	_____
– 5 dB	_____	– 5 dB	_____
– 10 dB	_____	– 10 dB	_____
– 20 dB	_____	– 20 dB	_____
– 30 dB	_____	– 30 dB	_____
– 40 dB	_____	– 40 dB	_____
– 50 dB	_____	– 50 dB	_____
– 60 dB	_____	– 60 dB	_____

Input Gain Accuracy

Channel 1

Attenuator Setting	FULL SCALE Setting	Measurement	Correction Factor	Result
20-0-0-0-0-0	0 dB	_____	0	_____
	+ 5 dB	_____	0	_____
	+ 10 dB	_____	0	_____
	+ 15 dB	_____	0	_____
	+ 20 dB	_____	0	_____
20-0-0-0-0-5	– 5 dB	_____	_____	_____
20-0-0-0-10-0	– 10 dB	_____	_____	_____
20-0-0-0-10-5	– 15 dB	_____	_____	_____
20-20-0-0-0-0	– 20 dB	_____	_____	_____
20-20-0-0-0-5	– 25 dB	_____	_____	_____
20-20-0-0-10-0	– 30 dB	_____	_____	_____
20-20-0-0-10-5	– 35 dB	_____	_____	_____
20-20-20-0-0-0	– 40 dB	_____	_____	_____
20-20-20-0-0-5	– 45 dB	_____	_____	_____
20-20-20-0-10-0	– 50 dB	_____	_____	_____
20-20-20-0-10-5	– 55 dB	_____	_____	_____
20-20-20-20-0-0	– 60 dB	_____	_____	_____

Table 5-6. Conformance Test Report (Continued)

Input Gain Accuracy

Channel 2

Attenuator Setting	FULL SCALE Setting	Measurement	Correction Factor	Result
20-0-0-0-0-0	0 dB	_____	0	_____
	+5 dB	_____	0	_____
	+10 dB	_____	0	_____
	+15 dB	_____	0	_____
	+20 dB	_____	0	_____
20-0-0-0-0-5	−5 dB	_____	_____	_____
20-0-0-0-10-0	−10 dB	_____	_____	_____
20-0-0-0-10-5	−15 dB	_____	_____	_____
20-20-0-0-0-0	−20 dB	_____	_____	_____
20-20-0-0-0-5	−25 dB	_____	_____	_____
20-20-0-0-10-0	−30 dB	_____	_____	_____
20-20-0-0-10-5	−35 dB	_____	_____	_____
20-20-20-0-0-0	−40 dB	_____	_____	_____
20-20-20-0-0-5	−45 dB	_____	_____	_____
20-20-20-0-10-0	−50 dB	_____	_____	_____
20-20-20-0-20-5	−55 dB	_____	_____	_____
20-20-20-20-0-0	−60 dB	_____	_____	_____

Output Gain Accuracy

Channel	Result
1	_____
2	_____

Table 5-6. Conformance Test Report (Continued)

Cutoff Frequency Accuracy

Channel 1

CUTOFF FREQ Setting	Result
800 Hz	_____
1 kHz	_____
1.1 kHz	_____
1.2 kHz	_____
1.4 kHz	_____
1.8 kHz	_____
8 kHz	_____
20 kHz	_____
40 kHz	_____
50 kHz	_____

Channel 2

CUTOFF FREQ Setting	Result
800 Hz	_____
1 kHz	_____
1.1 kHz	_____
1.2 kHz	_____
1.4 kHz	_____
1.8 kHz	_____
8 kHz	_____
20 kHz	_____
40 kHz	_____
50 kHz	_____

Passband Flatness/Amplitude Matching

Instrument Setting	Analyzer Settings			Results (dB p-p)		
				Passband Flatness		
CUTOFF FREQ	FREQ SPAN/DIV	RESOLUTION BANDWIDTH	SWEEP TIME/DIV	Channel 1	Channel 2	Amplitude Matching (Model 552A Only)
500 Hz	50 Hz	10 Hz	1 sec	_____	_____	0-400 Hz = _____ >400-500Hz _____
1 kHz	100 Hz	30 Hz	.2 sec	_____	_____	0-800 Hz = _____ >800-1 kHz _____
10 kHz	1 kHz	100 Hz	.2 sec	_____	_____	0-8 kHz = _____ >8-10 kHz _____
Low pass filter 50 kHz	5 kHz	300 Hz	.2 sec	_____	_____	0-40 kHz = _____ >40-50 kHz _____
High pass filter 30 kHz						

Table 5-6. Conformance Test Report (Continued)

Stop Band Attenuation

Channel 1				Channel 2			
Signal Source Frequency				Signal Source Frequency			
Low Pass Filter	High Pass Filter	CUTOFF FREQ Setting	Result	Low Pass Filter	High Pass Filter	CUTOFF FREQ Setting	Result
2.56 kHz	390 Hz	1 kHz	_____	2.56 kHz	390 Hz	1 kHz	_____
25.6 kHz	3.9 kHz	10 kHz	_____	25.6 kHz	3.9 kHz	10 kHz	_____

Harmonic Distortion

Channel	Result
1	_____
2	_____

Intermodulation Distortion (Model 552A only)

Channel	Result
1	_____
2	_____

Line Related Spurs

Channel 1

FULL SCALE Setting	Result
– 20 dB	_____
– 30 dB	_____
– 40 dB	_____
– 50 dB	_____
– 55 dB	_____
– 60 dB	_____

Channel 2

FULL SCALE Setting	Result
– 20 dB	_____
– 30 dB	_____
– 40 dB	_____
– 50 dB	_____
– 55 dB	_____
– 60 dB	_____

Table 5-6. Conformance Test Report (Continued)

Phase Matching (Model 552A Only)

Signal Source Frequency	CUTOFF FREQ Setting	Result
80 Hz	100 Hz	_____
100 Hz	100 Hz	_____
400 Hz	500 Hz	_____
500 Hz	500 Hz	_____
800 Hz	800 Hz	_____
1 kHz	1 kHz	_____
4 kHz	5 kHz	_____
5 kHz	5 kHz	_____
8 kHz	10 kHz	_____
10 kHz	10 kHz	_____
16 kHz	20 kHz	_____
20 kHz	20 kHz	_____
32 kHz	40 kHz	_____
40 kHz	40 kHz	_____
40 kHz	50 kHz	_____
50 kHz	50 kHz	_____

Noise Floor

Channel 1

FULL SCALE Setting	Result
+ 20 dB	_____
– 60 dB	_____

Channel 2

FULL SCALE Setting	Result
+ 20 dB	_____
– 60 dB	_____

5.4 CALIBRATION

Calibration of either channel or the entire instrument need only be done of it has failed the conformance test or been repaired. Before starting this test, list data errors (paragraph 5.2) caused by the external attenuator.

5.4.1 Factory Calibration

Wavetek maintains a factory repair department for those customers not possessing the necessary personnel or test equipment to calibrate the instrument. If the instrument must be returned to the factory, refer to paragraph 5.5.1 for address and instructions.

5.4.2 Required Test Equipment

Table 5-7 lists the test equipment required to perform the calibration procedure in table 5-8.

Table 5-7. Required Test Equipment

Equipment	Quantity	Specifications	Suggested Equipment
Oscilloscope	1	Dual channel, ⩾ 20 MHz bandwidth, external trigger input	
DVM	1	True RMS, 4½ digit resolution	Fluke Model 8050A
Spectrum Analyzer	1	To 50 kHz	Hewlett Packard Model 3580A
Phase Meter	1	1 MHz Bandwidth 0.05° Accuracy 0.01° Resolution	Dranetz Chassis: Model 305C/102,107 MOD 14 Module: 305-PA-3009
Signal Source	1	100 Hz to 50 kHz sine wave at 1 mV to 1 Vrms	Wavetek Model 5100
Low Noise Signal Source	1	All harmonic components – 80 dB below fundamental	Hewlett Packard Model 239
Coaxial Cables	4	BNC male connectors, RG-58U cable	
BNC Tee	1	1 male to 2 female connection	
Resistor	2	1kΩ, 1/4W	

Spectrum Analyzer Initial Settings:

DISPLAY	CLEAR WRITE	START/CTR	START
POWER	ON	FREQUENCY FINE (Vernier)	000
ADAPTIVE SWEEP	OFF	RESOLUTION BANDWIDTH	300 Hz
AMPLITUDE MODE	1 dB/Div (LOG)	DISPLAY SMOOTHING	MIN
AMPLITUDE REFERENCE LEVEL	NORMAL, dBV/LIN	FREQ SPAN/DIV	50 Hz
INPUT SENSITIVITY	0 dBV	SWEEP TIME/DIV	.2 sec
INPUT SENSITIVITY VERNIER	Fully cw (CAL)	SWEEP MODE	LOG

5.4.3 Calibration

WARNING

With the covers removed, dangerous voltage points may be exposed. Contact with any of these points could cause serious injury or death.

NOTE

Before removing the cover, disconnect the instrument from the ac power source. Refer to section 2 for cover removal procedure.

NOTE

The completion of the calibration procedure returns the instrument to correct alignment. ***CALIBRATION LIMITS AND TOLERANCES ARE NOT INSTRUMENT SPECIFICATIONS.*** *Instrument specifications are given in Section 1 of this manual.*

Instrument Initial Settings:

Channel Select	Both channels
FULL SCALE	0dBV
CUTOFF FREQ	10X1kHz
Output Gain	0 dB
AC/DC Coupling	DC
Digital Common (Rear Panel)	Earth/Chassis
Analog Common (Rear Panel)	Earth/Chassis

Connect the instrument to the ac power source and allow it to warm up at least 30 minutes for final calibration. Keep the instrument cover on to maintain heat, lifting only when making adjustments or measurements.

Perform calibration as per table 5-8. Figure 5-4 shows mainboard calibration points.

Table 5-8. Calibration Procedure

Step	Check	Tester	Tester Setting	Test Point	Instrument Setting	Adjust	Desired Result	Remarks
1	Power Supply	DVM	DC	U56 pin 20	See paragraph 5.4.3	Verify only	+5 ± 0.2V	Connect ground lead to TP9.
2				U8 pin 20				
3				U32 pin 20				
4				U14 pin 4			+13.0 ±1.5V	
5				U14 pin 11			−13.0 ±1.5V	
6				C159 + lead			+10 to −15V	
7				C161 − lead			−10 to −15V	
8	Signal levels	Scope	AC, .5V/div, .2 ms/div	TP1			≅3.5 Vp-p sine wave	Inject 2Vp-p 1kHz sine wave at Input 1 and Input 2 from signal source.
9				TP2				
10				TP6				
11				TP7				Move ground lead to TP11 or TP12.

Table 5-8. Calibration Procedure (Continued)

Step	Check	Tester	Tester Setting	Test Point	Instrument Setting	Adjust	Desired Result	Remarks
12	Signal levels	Scope	AC, .5V/div, .2 ms/div	TP3	See paragraph 5.4.3	Verify only	≅2Vp-p sine wave	See previous page
13				TP8				
14				Output 1				
15				Output 2				
16			.2 V/div	E1			≅0.9Vp-p sine wave	
17				E8				
18	DC Zero	DVM	DC	TP1		R11	0 ± 1.0mV	Remove injected signal.
19				TP6		R123		
20				TP2		R15	0 ± 0.5mV	Short Input 1 and Input 2 to ground.
21				TP3		R28		
22	(Model 552A only)			E1		R273 (DC Adj)		
23	DC Zero	DVM	DC	Output 1		R108		
24				TP7		R126		
25				TP8		R140		
26				E8		R274 (DC Adj)		
27				Output 2		R220		

Remove shorts from Input 1 and Input 2 connectors. Jumper a coaxial cable from the analyzer rear panel TRACKING OSCILLATOR OUT connector to the analyzer front panel INPUT connector. Adjust the LEVEL control (on the analyzer rear panel) for a display of − 1dBV. Remove cable from the analyzer INPUT and connect it to the Model 552A/553A Input 1 and Input 2 connectors.

NOTE

If adjustments to C2, C4, C66 or C68 must be made in the following steps, remove the metal shield(s) by first removing two screws at the top of the shield.

Table 5-8. Calibration Procedure (Continued)

Step	Check	Tester	Tester Setting	Test Point	Instrument Setting	Adjust	Desired Result	Remarks
28	Flatness	Spectrum Analyzer	See paragraph 5.4.2	E1	See paragraph 5.4.3	C4	Flattest trace	Store calibrated trace
29				E8		C68	Match with stored trace	
30			INPUT SENSITIVITY: −20 dBV	E1	FULL SCALE: +20 dBV	C2		May need to adjust INPUT SENSITIVITY VERNIER.
31				E8		C66		After completing step 31, deselect STORE.
Steps 32 through 41 describe filter alignment for both Channel 1 and Channel 2. References to Channel 2 in these and subsequent steps are shown within parenthesis ( ). Perform the entire filter alignment for Channel 1, then return to step 32 and align Channel 2.								
32	Filter Alignment	DVM	AC, Volts	E6 (E13)	FULL SCALE: 0 dBV	C31 (C93)	Low pass filter; 0.317 ±0.01 Vrms High pass filter; 0.305 ±0.01 Vrms	Replace signal from from analyzer at Input 1 and Input 2 with 1V rms sine wave from signal source at 4.456 kHz for low pass filter, 22.44 kHz for high pass filter.
Remove the signal source output from the Input 1 (Input 2) connector. Disconnect the jumper from E6 (E13). Jumper a coaxial cable from the analyzer rear panel TRACKING OSCILLATOR OUT connector to the analyzer front panel INPUT connector. Set the spectrum analyzer INPUT SENSITIVITY to −10 dBV and INPUT SENSITIVITY VERNIER to CAL. Adjust the LEVEL control (on the analyzer rear panel) for a display of −14dBV. Move cable from the analyzer INPUT to the right side of E6 (E13) on the instrument.								
33		Spectrum Analyzer	INPUT SENSITIVITY: 0 dBV, SWEEP MODE: "REP", FREQUENCY FINE (vernier) to center trace on display	TP4 (TP5)	CUTOFF FREQ: 10X100Hz	R56 (R200)	See figure 5-1	Use INPUT SENSITIVITY VERNIER to set and maintain top of trace at −2 dB. Press STORE when desired results is obtained.

Table 5-8. Calibration Procedure (Continued)

NOTE

In the remaining steps, do not move FREQUENCY FINE or INPUT SENSITIVITY verniers unless instructed to do so.

Step	Check	Tester	Tester Setting	Test Point	Instrument Setting	Adjust	Desired Result	Remarks
34	Filter Alignment (Cont)	Spectrum Analyzer	FREQUENCY FINE (vernier): ≅34 kHz FREQUENCY SPAN/DIV: 2 kHz	TP4 (TP5)	CUTOFF FREQ: 40X1kHz	C52 (C114)	Tops overlapped	Use FREQUENCY FINE (vernier) to bring together center of current and stored traces.
35			INPUT SENSITIVITY: −20 dBV, Deselect STORE, FREQ SPAN/DIV: .1 kHz for low pass filter; .2 kHz for high pass filter, FREQUENCY FINE (Vernier): Center trace on display (≅0 Hz)	U14 pin 7 (U37 pin 7)	CUTOFF FREQ: 10X100Hz	R82 (R210)	See figure 5-2	Disconnect jumper from E7 (E14). Move analyzer rear panel TRACKING OSCILLATOR OUT signal to front of E7 (E14). Use INPUT SENSITIVITY VERNIER to set and maintain top of trace at −2 dB. Press STORE when desired result is obtained.
36			FREQ SPAN/DIV: 5 kHz		CUTOFF FREQ: 50X1kHz for low pass filter; 25X1kHz for high pass filter	C55 (C117)	Merge top of current and stored traces	Use FREQUENCY FINE vernier to merge center of trace (≅10 kHz).

Table 5-8. Calibration Procedure (Continued)

Move coaxial cable from E7 (E14) to analyzer front panel INPUT connector. Deselect STORE, set the spectrum analyzer INPUT SENSITIVITY to 0 dBV and INPUT SENSITIVITY VERNIER to CAL. Adjust the LEVEL control (on the analyzer rear panel) for a display of 0dBV. Remove cable from the analyzer INPUT and connect it to the Model 552A/553A Input 1 (Input 2) connector.

Step	Check	Tester	Tester Setting	Test Point	Instrument Setting	Adjust	Desired Result	Remarks
37	Filter Alignment (Cont)	Spectrum Analyzer	FREQ SPAN/DIV: .1 kHz for low pass filter; .2 kHz for high pass filter, FREQUENCY FINE (Vernier): ≅0 Hz	Output 1 (Output 2)	CUTOFF 10X100 Hz	Right side of trace: R56 (R200) Top of trace: R82 (R210)	≤0.5 dB p-p ripple	Connect E6 (E13) and E7 (E14) jumpers. Use FREQUENCY FINE vernier to move first hump to center (vertical) line of display. Press STORE when desired result is obtained.
38			FREQ SPAN/DIV: 1 kHz for low pass filter; 2 kHz for high pass filter		CUTOFF FREQ: 10X1kHz	Right side of trace: C40 (C102) Top of trace: C49 (C111) Overall slope: C31 (C93)	Match with stored trace	Use FREQUENCY FINE vernier to overlap traces. Slight adjustment of C52 (C114) may be necessary. Maintain trace stored from step 37.
39			FREQ SPAN/DIV: 5 kHz, FREQUENCY FINE (vernier) ≅5 kHz		CUTOFF FREQ: 50X1 kHz for for low pass filter; 25X1kHz for for high pass filter	Right side of trace: C52 (C114) Top of trace: C55 (C117)	Match with trace stored in step 37	Use FREQUENCY FINE vernier to overlap traces. When desired result is obtained, deselect STORE, then STORE this trace.

Table 5-8. Calibration Procedure (Continued)

Step	Check	Tester	Tester Setting	Test Point	Instrument Setting	Adjust	Desired Result	Remarks
40	Filter Alignment (Cont)	Spectrum Analyzer	INPUT SENSITIVITY: – 20 dBV	Output 1 (Output 2)	FULL SCALE: + 20dBV	Verify only	Verify current trace characteristics match stored trace	INPUT SENSITIVITY VERNIER may be used to overlap traces. Maintain trace stored in step 39.

Move coaxial cable from Model 552A/553A Input connector to analyzer front panel INPUT connector. Set the spectrum analyzer INPUT SENSITIVITY to – 30 dBV and INPUT SENSITIVITY VERNIER to CAL. Adjust the LEVEL control (on the analyzer rear panel) for a display of – 30dBV. Remove cable from the analyzer INPUT and return it to the Model 552A/553A Input 1 (Input 2) connector.

41			INPUT SENSITIVITY: 0dBV		FULL SCALE: – 30 dBV		Verify current trace characteristics match stored trace and OVLD indicator not flashing	INPUT SENSITIVITY VERNIER may be used to overlap traces. When desired result obtained, deselect STORE.

If the Channel 2 filter has not yet been aligned, return to step 32 after making the following spectrum analyzer and instrument setting changes.

Spectrum Analyzer Settings:

INPUT SENSITIVITY	– 20 dBV
FREQUENCY FINE (Vernier)	000
FREQ SPAN/DIV	50 Hz
SWEEP MODE	LOG

Instrument Settings:

FULL SCALE	0dBV
CUTOFF FREQ	10X1kHz

Use TP11 or TP12 as the ground reference point for internal measurements.

42	Gain Adjustment	DVM		Output 1, then Output 2	CUTOFF FREQ: 10X100Hz for low pass filter; 10X10 Hz for high pass filter, FULL SCALE: 0 dBV	R103 (R215)	1.0 ± 0.1mVrms Verify OVLD indicator not flashing	Replace analyzer signal with 100 Hz (1000 Hz for high pass filter) 1Vrms sine wave at both Input 1 and Input 2.

Remove signal from Input 1 and Input 2. Set the spectrum analyzer INPUT SENSITIVITY VERNIER to CAL. For Model 553A only, set spectrum analyzer FREQUENCY FINE vernier to ≅0 kHz, then skip to step 47.

For Model 552A only, jumper a coaxial cable from the analyzer rear panel TRACKING OSCILLATOR OUT connector to the analyzer front panel INPUT connector. Adjust the LEVEL control (on the analyzer rear panel) for a display of 0 dBV. Remove cable from the analyzer INPUT and connect it to both Model 552A Input 1 and Input 2 connectors.

Table 5-8. Calibration Procedure (Continued)

Step	Check	Tester	Tester Setting	Test Point	Instrument Setting	Adjust	Desired Result	Remarks
43	Amplitude Match (Model 552A only)	Spectrum Analyzer		Output 1 and Output 2	CUTOFF FREQ: 50X1kHz	Verify only	Difference in amplitude between Output 1 and Output 2 ≤0.2 dB	Store channel 1, then compare with channel 2 for each of the three cutoff frequencies.
44			FREQ SPAN/DIV: 1 kHz		CUTOFF FREQ: 10X1kHz			
45			FREQ SPAN/DIV: .1 kHz		CUTOFF FREQ: 10X100Hz			

Deselect STORE. For the next step, table 5-9 is used to define the Model 552A CUTOFF FREQ, signal source frequency and specification. Make a copy of this table, then use it to record the phase meter readings. If any readings are not within specification, use it to help decide which reading to monitor when making adjustments.

46	Phase Match (Model 552 only)	Phase Meter	Slide switch to Φ ANGLE, Toggle switch up (>12 Hz)	Output 1 to REFERENCE INPUT Output 2 to SIGNAL INPUT	See Table 5-9	C40, C49, C102 and C111 equally to bring worst case just within specification	See Table 5-9	Replace signal from analyzer with 2Vp-p sine wave. Inject into Input 1 and Input 2 at frequencies listed in table 5-9.

Remove signal from Input 1 and Input 2. Set spectrum analyzer FREQUENCY FINE vernier to ≅0 kHz and Model 552A CUTOFF FREQ to 10X100 Hz. Jumper a coaxial cable from the analyzer rear panel TRACKING OSCILLATOR OUT connector to the Model 552A Input 1 and Input 2 connectors. Verify ripple (step 37) has remained within specification for both channels but do not STORE the result. After verifying step 37, remove the analyzer signal from Input 1 and Input 2 connectors, then move to step 47.

47	Stop Band Attenuation	Spectrum Analyzer	FREQ SPAN/DIV: .5 kHz for low pass filter; 2 kHz for high pass filter	Output 1	CUTOFF FREQ: 10X1kHz for low pass filter; 10X100 Hz for high pass filter	Amplitude of injected signal	Top of trace at top display line	Inject 2.56 kHz (3.9 kHz for high pass filter) ≅2Vp-p sine wave into Input 1.
48			INPUT SENSITIVITY: −70 dBV		CUTOFF FREQ: 10X100Hz for low pass filter; 10X1 kHz for high pass filter	Verify only	Top of trace at or below −2 dB line on display	
49			FREQ SPAN/DIV: 2 kHz for low pass filter; .2kHz for high pass filter, START/CTR: CTR FREQUENCY FINE (vernier) ≈25kHz, RESOLUTION BANDWIDTH (high pass filter only) 30 Hz		CUTOFF FREQ: 10X1kHz for low pass filter; 10X100Hz for high pass filter			Change injected signal frequency to 25.6 kHz for low pass filter; 390 Hz for high pass filter.

Table 5-8. Calibration Procedure (Continued)

Step	Check	Tester	Tester Setting	Test Point	Instrument Setting	Adjust	Desired Result	Remarks
50	Stop Band Attenuation	Spectrum Analyzer	FREQ SPAN/DIV: .5 kHz INPUT SENSITIVITY: 0 dBV, FREQUENCY FINE (vernier) ≈2.5kHz	Output 1	CUTOFF FREQ: 10X1kHz for low pass filter; 10X100Hz for high pass filter	Amplitude of injected signal	Top of trace at top display line	Inject 2.56 kHz ≅2Vp-p sine wave into Input 2.
51			INPUT SENSITIVITY: −70dBV		CUTOFF FREQ: 10X100Hz	Verify only	Top of trace at −2 dB line on display	
52			FREQ SPAN/DIV: 2 kHz, FREQUENCY FINE (vernier) ≅25 kHz		CUTOFF FREQ: 10X1kHz			Change injected sig-frequency to 25.6 kHz. After Desired Result obtained, remove signal at Input 2.
53	Full Scale Verification	DVM	AC Volts	DVM	CUTOFF FREQ: 10X10 Hz for high pass filter; 10X1kHz for low pass filter	Amplitude of injected signal	0.3 Vrms	Inject 1kHz sine wave through attenuator to DVM. After Desired Result achieved, set dB/Volt switch to dB, push DVM RELATIVE button "out" then "in" to zero meter.
		Attenuator	20-0-0-0-0-0					
54		DVM, Attenuator Oscilloscope		Output 1 and Output 2		Verify only	0 ± 0.2 dB Normal signal integrity for all FULL SCALE settings in steps 55 through 70	Move attenuator output from DVM to Input 1 and Input 2. "T" output to DVM and scope.
55					FULL SCALE: +5 dBV		−5 ± 0.2 dB	Copy Input Gain Accuracy chart (table 5-6) for channels 1 and 2. Remarks cont. on next page.
56					FULL SCALE: +10 dBV		−10 ± 0.2 dB	

Table 5-8. Calibration Procedure (Continued)

Step	Check	Tester	Tester Setting	Test Point	Instrument Setting	Adjust	Desired Result	Remarks
57	Full Scale Verification (Cont)	DVM, Attenuator, Oscilloscope	20-0-0-0-0-0	Output 1 and Output 2	FULL SCALE: +15 dBV	Verify only	−15 ±0.2 dB	Verify and record on chart (table 5-6) steps 54 throught 70 for both channels Add or subtract attenuator Correction Factor (paragraph 5.2.2) to obtain the correct Result
58					FULL SCALE: +20 dBV		−20 ±0.2 dB	
59			20-0-0-0-0-5		FULL SCALE: −5 dBV		0 ±0.2 dB	
60			20-0-0-0-10-0		FULL SCALE: −10 dBV			
61			20-0-0-0-10-5		FULL SCALE: −15 dBV			
62			20-20-0-0-0-0		FULL SCALE: −20 dBV			
63			20-20-0-0-0-5		FULL SCALE: −25 dBV			
64			20-20-0-0-10-0		FULL SCALE: −30 dBV			
65			20-20-0-0-10-5		FULL SCALE: −35 dBV			
66			20-20-20-0-0-0		FULL SCALE: −40 dBV			
67			20-20-20-0-0-5		FULL SCALE: −45 dBV			
68			20-20-20-0-10-0		FULL SCALE: −50 dBV			
69			20-20-20-0-10-5		FULL SCALE: −55 dBV			
70			20-20-20-20-0-0		FULL SCALE: −60 dBV			

Table 5-8. Calibration Procedure (Continued)

Step	Check	Tester	Tester Setting	Test Point	Instrument Setting	Adjust	Desired Result	Remarks
71	Harmonic Distortion	Low Noise Signal Source, Spectrum Analyzer	INPUT SENSITIVITY: 0 dBV, AMPLITUDE MODE: 10dB/DIV. FREQUENCY FINE (vernier) ≅5 kHz, FREQ SPAN/DIV: 1 kHz, RESOLUTION BANDWIDTH: 100 Hz	Output 1 and Output 2	CUTOFF FREQ: 50X1kHz for low pass filter; 10X10 Hz for high pass filter FULL SCALE: 0 dBV	Verify only	Second harmonic < – 72dB	Inject 1kHz 0 dBV sine wave at Input 1 and Input 2. Verify steps 71 through 75 for channel 1, then channel 2.
72					FULL SCALE. – 30 dBV			Change amplitude to – 30 dBV.
73					FULL SCALE: – 40 dBV			Change amplitude to – 40 dBV.
74					FULL SCALE: – 50 dBV			Change amplitude to – 50 dBV.
75					FULL SCALE: – 60 dBV			Change amplitude to – 60 dBV.
76	Intermodulation Distortion (Model 552A only. For Model 553A, skip to step 79.)	Signal Sources (2), Spectrum Analyzer	AMPLITUDE MODE: 1 dB/DIV		CUTOFF FREQ: 20X1kHz, FULL SCALE: 0 dBV	Signal source output voltages and frequencies	Both peaks at – 6 dBV	Connect equipment as shown in figure 5-3. Verify steps 76 through 78 for channel 1, then channel 2.
77			AMPLITUDE MODE: 10 dB/DIV			Verify only	5 kHz tone < – 75 dBV	Change signal source "A" output to 35 kHz and signal source "B" output to 40 kHz.
78					FULL SCALE: – 30 dBV			Lower signal source amplitudes to – 36 dBV.

Table 5-8. Calibration Procedure (Continued)

Step	Check	Tester	Tester Setting	Test Point	Instrument Setting	Adjust	Desired Result	Remarks
79	Line Related Spurious	Spectrum Analyzer	INPUT SENSITIVITY: −70 dBV, AMPLITUDE MODE: 1dB/DIV, SWEEP TIME/DIV: .5 sec, RESOLUTION BANDWIDTH: 10 Hz, FREQ SPAN/DIV 20 Hz, FREQUENCY FINE (vernier) 0 Hz	Output 1 and Output 2	CUTOFF FREQ: 1X10 Hz for high pass filter; 20X1kHz for low pass filter, FULL SCALE: −20 dBV	Verify only	60, 120 and 180 Hz spurs < −72 dBV	Disconnect signals from Input 1 and Input 2, then short their center conductors to ground. Verify steps 79 through 84 for channel 1, then channel 2.
80					FULL SCALE: −30 dBV			
81					FULL SCALE: −40 dBV			
82					FULL SCALE: −50 dBV			
83					FULL SCALE: −55 dBV		60, 120 and 180 Hz spurs < −60 dBV	
84					FULL SCALE: −60 dBV			
85	Noise Floor	RMS voltmeter			CUTOFF FREQ: 50X1kHz for low pass filter; 1X10 Hz for high pass filter, FULL SCALE: +20 dBV		<1.0 mVrms for low pass pass filter; <6 mVrms for high pass filter (Channel 1, then channel 2)	After step 85 is complete, disconnect Input 1 and Input 2 shorts.
86	LCD Adjust	N/A	N/A	Front Panel	N/A	R12 (Front panel)	Adjust for a sharp display when viewed at (and somewhat above) horizontal plane of instrument. Also adjust for minimum segment bleed through when viewed from each side.	

Table 5-9. Phase Meter Readings (Reproducible)

Instrument CUTOFF FREQ	Signal Source Frequency (Hz)	Phase Meter Reading	Specification
10 X 100 Hz	100		±1°
	200		
	300		
	400		
	500		
	600		
	700		
	800		
	900		±2°
	950		
	1 k		
10 X 1 kHz			±1°
	2 k		
	3 k		
	4 k		
	5 k		
	6 k		
	7 k		
	8 k		
	9 k		±2°
	9.5 k		
	10 k		
50 X 1 kHz			±1°
	20 k		
	30 k		
	40 k		
	45 k		±2°
	50 k		

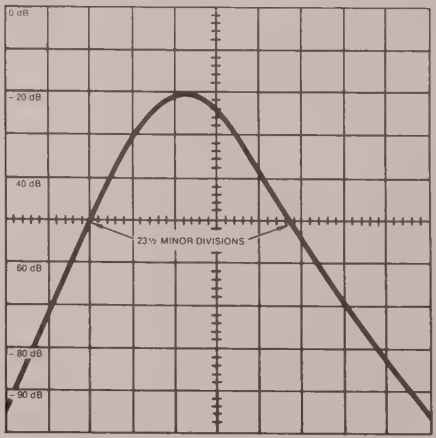


Figure 5-1. Desired Results for Calibration Procedure Step 33

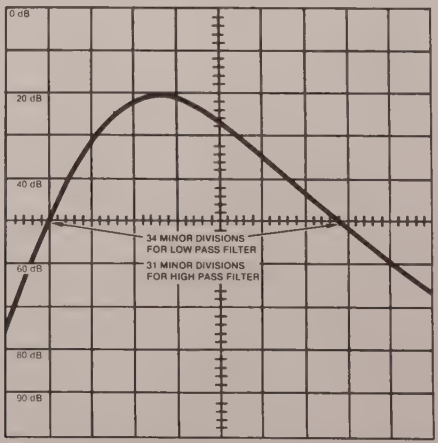


Figure 5-2. Desired Results for Calibration Procedure Step 35

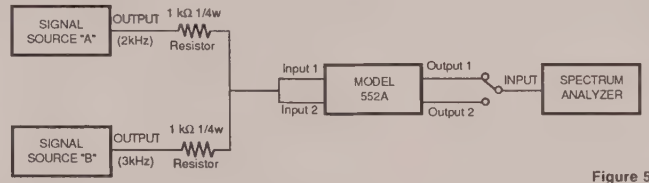


Figure 5-3. Instrument Connections for Calibration Procedure Steps 76 Through 78 (Model 552A Only)

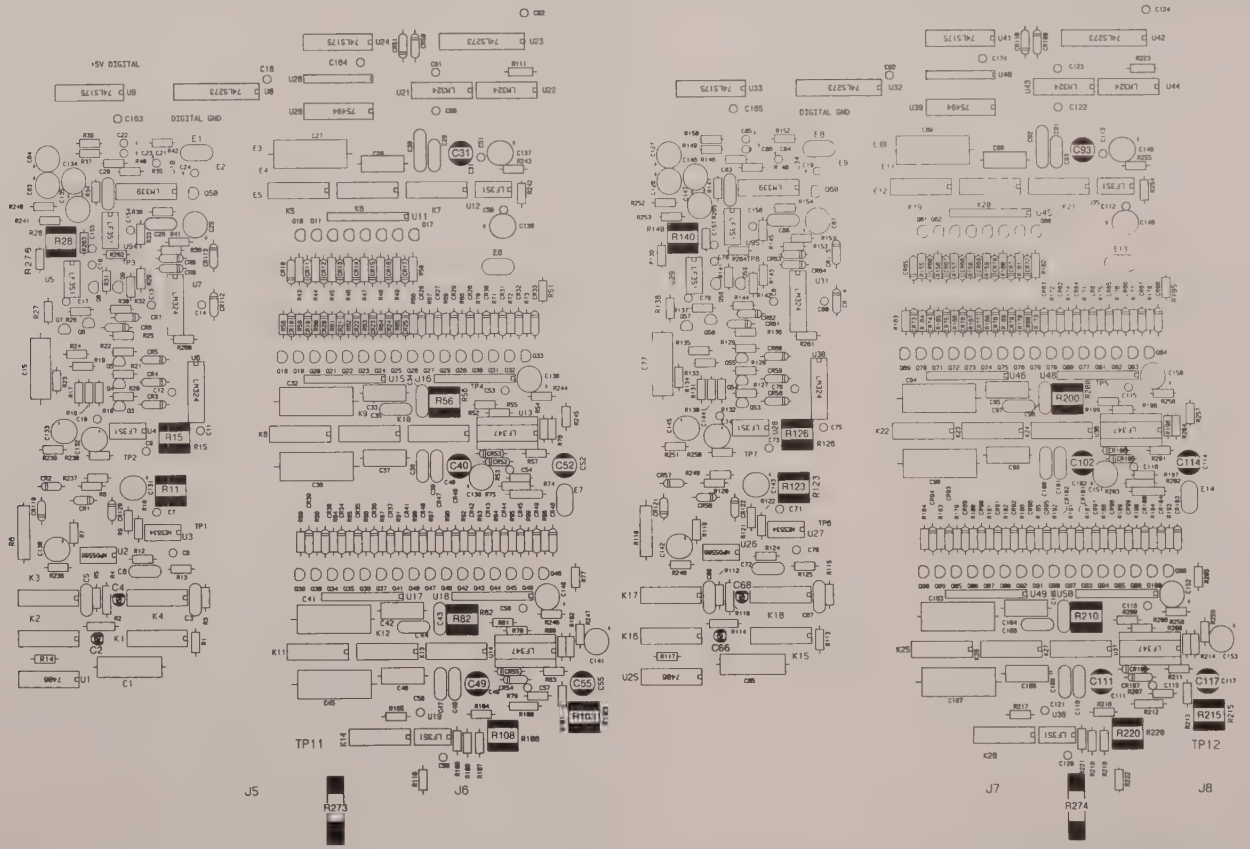


Figure 5-4. Mainboard Calibration Points

5.5 TROUBLESHOOTING

5.5.1 Factory Repair

Wavetek maintains a factory repair department for those customers not possessing the necessary personnel or test equipment to maintain the instrument. If an instrument is returned to the factory for calibration or repair, a detailed description of the specific problem and any related symptoms should be attached to the instrument. Before returning a unit to the factory, authorization from Customer Service must be obtained by calling or writing to:

Customer Service
Wavetek San Diego, Inc.
9045 Balboa Ave.
San Diego, CA 92123
Telephone: (619) 279-2200
TWX: (910) 335-2007

5.5.2 Before You Start

Since no troubleshooting guide can possibly cover all the potential problems, the aim of this guide is to give a methodology which, if applied consistently, will lead to the problem area. Therefore, it is necessary to familiarize yourself with the instrument by reviewing the circuit description (section 4) in conjunction with the schematics (section 6). Successful troubleshooting depends upon understanding the circuit operation within each functional block as well as the block relationships.

WARNING

With the covers removed, dangerous voltage points may be exposed. Contact with any of these points could cause serious injury or death.

The intent of this section is to provide the information required to return the instrument to proper operation. Information is divided into two parts. Part one (table 5-10) contains a list of symptoms that should be useful in determining which circuit within the instrument is defective. Part two consists of circuit guides which include settings and measurements for troubleshooting an individual block. Each circuit guide also references related schematics and circuit descriptions. Table 5-11 provides a list of these circuit guides.

Before beginning the troubleshooting process, verify the instrument's controls are set correctly. For more information about instrument operation, refer to section 3 of this manual.

Also, try to rule out calibration as a possible problem. For instance, if the amplitudes at Output 1 and Output 2 on the Model 552A do not match, even though all instrument settings for both channels are identical and the same signal is injected at both input connectors, then gain trim pots R103 (channel 1) or R215 (channel 2) may need adjustment.

Finally, inspect the instrument's components, wiring, and circuit boards for heat damage.

5.5.3 Isolating a Problem

To successfully troubleshoot this instrument, the symptom must first be identified, the faulty block isolated, the block analyzed, and the defective component located and replaced.

A minimum of interior measurements need be taken to identify the symptom and isolate the circuit block causing the problem. This can be done by combining table 5-10 with an effective use of all the front panel controls.

Because both channels in the Model 552A are identical, and those in the Model 553A are substantially similar, it may be wise to use one channel as a model for troubleshooting the second. To accomplish this, inject identical signals to Input 1 and Input 2 connectors and duplicate instrument settings (use "both channel" mode described in paragraph 3.3.1).

NOTE

Most channel 2 component designations are shown within parenthesis.

Once the block is isolated, refer to the appropriate circuit guide (table 5-11) and take the measurements given to check out the block. Paragraph 5.5.5 gives component troubleshooting information.

Table 5-10. Fault Isolation

Primary Indication	Initial Examination	Probable Cause
Front panel display or LED's not normal	Output 1 (Output 2) signal normal	Front panel display (paragraph 5.5.4.4), LED (paragraph 5.5.4.5).
	Output 1 (Output 2) signal not normal.	Ribbon cable, front panel key(s) (paragraph 5.5.4.3, digital control section (paragraph 5.5.4.1).

Table 5-10. Fault Isolation (Continued)

Primary Indication	Initial Examination	Probable Cause
Incorrect IEEE-488 or RS-232-C interfacing	Unit works normally under front panel control.	Programming error (paragraphs 3.4.1 through 3.4.1.12 for IEEE-488 or 3.4.2 through 3.4.2.12 for RS-232-C), hardware failure (paragraph 5.5.4.7 for IEEE-488 or 5.5.4.6 for RS-232-C).
	Unit not working normally under front panel control.	Digital Control (Microprocessor circuitry) paragraph 5.5.4.1.
Incorrect Output 1 (Output 2) signal	Perform only calibration step 16 (17) to check signal at E1 (E8) and U14 (U37) pin 14.	E1 (E8) not normal: refer to paragraph 5.5.4.8.
		E1 (E8) normal, but U14 (U37) pin 14 not approximately 650 mVp-p: refer to paragraph 5.5.4.9.
	If signals are only slightly abnormal, do the entire calibration procedure.	E1 (E8) and U14 (U37) pin 14 both normal: refer to paragraph 5.5.4.10.
Incorrect overload (OVLD) indication		Overload circuit (paragraph 5.5.4.11).

5.5.4 Troubleshooting Guides

Table 5-11. Circuit Block Guides

Circuit Guide	Paragraph
Digital Control (Microprocessor Circuitry)	5.5.4.1
Amplifier/Filter Control	5.5.4.2
Keyboard	5.5.4.3
Display	5.5.4.4
LED's	5.5.4.5
RS-232-C Interface	5.5.4.6
IEEE-488 Interface	5.5.4.7
Amplifier/Attenuator	5.5.4.8
Filter	5.5.4.9
Output Amplifier	5.5.4.10
Overload Circuit	5.5.4.11
Power Supply	5.5.4.12
DC-DC Converter	5.5.4.13

5.5.4.1 Digital Control (Microprocessor Circuitry)

Related information in this manual.

Schematic: Model 552A; 0103-00-2364 Sheet 4.
Model 553A; 0103-00-2872 Sheet 4.

Circuit Description: Paragraph 4.2.4.

When the microprocessor and interface system is suspect, troubleshooting can be done by observing the symptoms to decide which checks will be used to locate a faulty digital circuit block. General techniques of troubleshooting digital systems are then applied to these blocks. One valuable technique involves using an oscilloscope to check for "stuck" bits on each line of a constantly varying address or data bus. A "stuck" bit may be constantly high, low, or tri-state (the output floats to a threshold level of 2 to 2.5V). It could also vary between a tri-state and a high or a low level without going to the third level. The cause of a "stuck bit" can be found by isolating IC pins and connectors from the line in question. If more than one line is "stuck", make a list of these lines and check for a common IC.

NOTE

When taking waveform readings in the digital control circuit, always use an X10 probe to prevent loading and reduce the amount of ringing.

To troubleshoot the Digital Control (Microprocessor Circuitry), do the following:

1. Verify U53 and U60 are firmly in their sockets.
2. Verify +5 V (power supply) at U53 pin 11. If not normal, refer to paragraph 5.5.4.12.
3. Check for clock signals at U52 (table 5-12).
4. Verify that at initial power up the reset ($\overline{RST}$) line at U53 pin 26 is a TTL low for at least 20 ms before going TTL high.
5. Verify input and output lines at U59 are normal (table 5-13).
6. Verify input and output lines at U71 (U70) are normal (table 5-14).

Table 5-12. Clock Signals

Test Point	Frequency	Approximate Positive Duty Cycle*
U52 pin 1	2.048 MHz	25%
U52 pin 3	1.024 MHz	50%
U52 pin 4	10.24 MHz	50% (Ringing usually visible)
U52 pin 13	102.4 kHz	50%

* All amplitudes approximately TTL levels.

Table 5-13. U59 Input and Output Line Status

Test Point	Before Interrupt	During Interrupt
U59 pin 1	Random TTL pulse pattern	Modified Random TTL pulse pattern
U59 pin 2	TTL Low	TTL high with $\overline{OVLD}$ $\overline{1}$ enabled
U59 pin 4		TTL high with RS-232-C enabled
U59 pin 11		TTL high with IEEE-488 enabled
U59 pin 13		TTL high with $\overline{OVLD}$ $\overline{2}$ enabled
U59 pin 15		TTL high with IEEE-488 "GET" enabled
U59 pin 17		TTL high with the keyboard enabled

Table 5-14. U71 (U70) Input and Output Line Status

Test Point	Normal	Overload (OVLD)*
U71 (U70) pin 2	+14.5V	−9.0V
U71 (U70) pin 4	+0.7V	+5.0V

* To obtain an "Overload Condition" for this test, increase the signal amplitude at AMP 1 to slightly outside the boundaries set by U10 (U34) pins 4 and 6.

5.5.4.2 Amplifier/Filter Control

Related information in this manual.
Schematic: Model 552A; 0103-00-2364 Sheet 5.
Model 553A; 0103-00-2872 Sheet 5.
Circuit Description: Paragraph 4.2.5.

To troubleshoot the Amplifier/Filter Control circuit, do the following:

1. Verify +5 V (power supply) at U90 pin 14. If not normal, refer to paragraph 5.5.4.12.
2. Press AC/DC Coupling button to verify the following:
   A) Input data lines (table 5-15).
   B) U93 pins 8, 10 and 12 (figure 5-5).
   C) U90 pins 3, 6, 8 and 11 are high unless a high at the appropriate output line from shift register U91 coincides with a load pulse from U93 pin 10. This forces the U90 output pin low for 0.6 ms.
3. Verify U91 pins 3, 4, 5 and 6, U92 pins 3, 4, 5, 6, 10, 11, 12 and 13 (shift register outputs) are TTL high or low depending upon the data held in these registers.

Table 5-15. Amplifier/Filter Input Data Lines

Test Point	Before Parameter Update	AC/DC Coupling Button Pressed
U86 pin 4 (D0/MLE)	Random TTL pulse pattern	Modified Random TTL pulse pattern
U86 pin 5 (D1/DATA OUT)		
U86 pin 9 ($\overline{WE}$)	Random +4 to +5 V pulse pattern	
U86 pin 12 (D2/SHIFT CLK)	Random TTL pulse pattern	

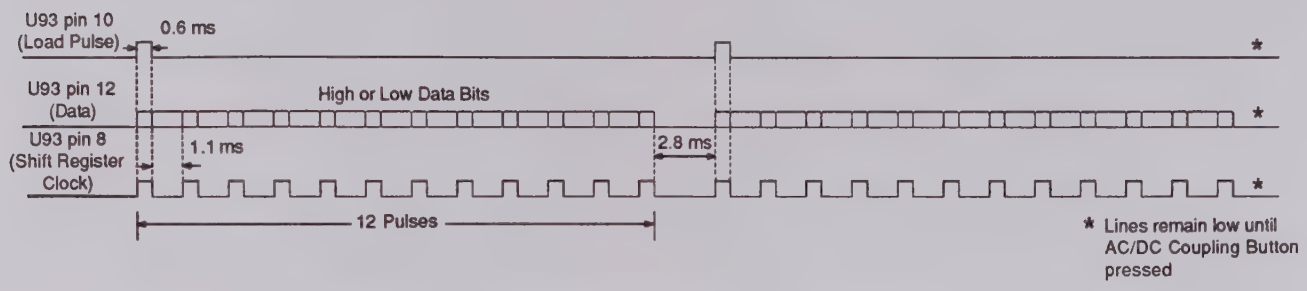


Figure 5-5. Amplifier/Filter Control Timing Diagram

5.5.4.3 Keyboard

Related information in this manual.
Schematic: 0103-00-2365 Sheet 1.
Circuit Description: Paragraph 4.3.

If, during the troubleshooting process, the problem is believed to be caused by a faulty key pad, short the runs to that key and see if the unit responds.

To troubleshoot the Keyboard circuitry, verify the following:

1. +5 V (power supply) at U1 pin 40. If not normal, refer to paragraph 5.5.4.12.
2. 1.024 MHz TTL level signal (50% duty cycle) at U1 pin 3 (CLK).
3. TTL low at U1 pin 4 (IRQ). Should go TTL high for at least 0.4 ms when a front panel button is pressed.
4. Random TTL pulse pattern at U1 pin 10 ($\overline{RD}$), pin 21 (Ao) and pin 22 ($\overline{CS}$). Pulse patterns are modified when a front panel button is pressed.
5. U7 pin 4 is TTL low. Pressing ↑ or ↓ causes the line to oscillate between TTL high for 200 ms and TTL low for 125 ms.
6. 1 kHz TTL level signal (50% duty cycle) at U7 pin 1.
7. 2 kHz TTL level signal (50% duty cycle) at U7 pin 2.
8. 4 kHz TTL level signal (50% duty cycle) at U7 pin 3.
9. U7 output lines (table 5-16).
10. U1 pins 1 (R2), 2 (R3), 5 through 8 (R4-R7), 38 (R0) and 39 (R1) are TTL high until a button connected to that line is pressed, then 0 to +5 V, 90% positive duty cycle, 1 kHz signal.

Table 5-16. U7 Output Lines

Test Point	Buttons Not Pressed	Buttons Pressed
U7 pin 13	0 to +4 V, 90% positive duty cycle, 1 kHz signal	Increases to +5 V when 1, 4, 7 or +/− buttons pressed
U7 pin 14		Increases to +5V when 0, 2, 3, 5, 6, 8, 9 or CLR buttons pressed
U7 pin 15	Lines remain high when ↑ or ↓ pressed	Increases to +5 V when 10 Hz, 100 Hz, 1 kHz, dBv, ↑ or ↓ buttons pressed

5.5.4.4 Display

Related information in this manual.
Schematic: 0103-00-2365 Sheet 1.
Circuit Description: Paragraph 4.3.

To troubleshoot the Display circuitry, verify the following:

1. Problem is not caused by an incorrect adjustment of R12 (final step in the calibration procedure).
2. +5 V (power supply) at U5 pin 7. If not normal, refer to paragraph 5.5.4.12.
3. U5 pins 8 (SCK), 9 (SI), 10 (CS) and 12 (C/$\overline{D}$) are TTL high and become random TTL pulse patterns when the display changes.
4. U5 pin 13 ($\overline{RESET}$) is TTL low for about 1 sec when unit turned on, then remains TTL high.

5. U5 pin 3 = +4 V, pin 4 = +3 V, and pin 5 = +2 V.
6. Approximately 525 kHz TTL level signal (55% positive duty cycle) at U5 pin 1 (CL2).
7. Ac coupled, 45% positive duty cycle version of pin 1 at U5 pin 52 (CL1).
8. U5 pin 11 TTL low. Becomes a random TTL pulse pattern when the display changes.
9. DS1 (DS2) pins 1, 2, 3, 5, 10, 12, 13, 15, 17, 18, 20, 21, 24, 27, 29, through 36 and 39 are 2 or 4 level random stair-steps. See figure 5-6 for pin locations.

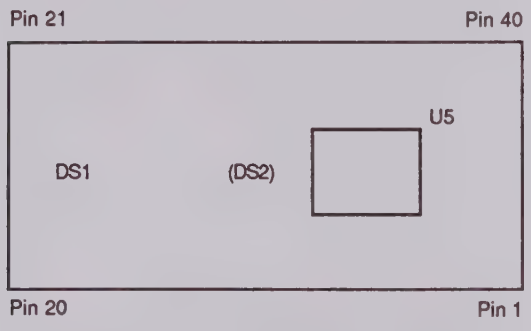


Figure 5-6. DS1 (DS2) Pin Location

5.5.4.5 LED's

Related information in this manual.
Schematic: 0103-00-2365 Sheet 1.
Circuit Description: Paragraph 4.3.

To troubleshoot the LED circuitry, check the following:

1. +5 V (power supply) at U3 pin 9. If not normal, refer to paragraph 5.5.4.12.
2. 500 Hz TTL level signal (50% duty cycle) at U2 pins 1 and 3.
3. Random and repeating TTL pulse pattern at U3 pins 1 through 8.
4. +5 V with sweeping negative slopes, sometimes reaching 0 V at U3 pins 11 through 18.
5. Open or shorted LED's CR1 through CR8.

5.5.4.6 RS-232-C Interface

Related information in this manual.
Schematic: Model 552A; 0103-00-2364 Sheet 4.
Model 553A; 0103-00-2872 Sheet 4.
Circuit Description: Paragraph 4.2.7

To troubleshoot the RS-232-C circuitry, do the following:

1. Check power supplies: +5 V at U68 pin 39; +9 to +15 V at U66 pin 14; −9 to −15 V at U66 pin 1. If +5V supply not normal, refer to paragraph 5.5.4.12. If U66 pin 1 or 14 not normal, refer to paragraph 5.5.13.
2. Verify a 2.048 MHz clock (25% positive duty cycle) at U68 pin 16 (CLK).
3. Verify TTL high with TTL low pulses every 1.5 ms at U69 pin 1.
4. Verify TTL high at U68 pin 14 (CS2).
5. Verify DIP switches (S2) and pull-up resistors U85) are working properly.

NOTE

The remaining steps relate to programming the instrument. Because remote problems are often caused by improper programming format, the user is instructed (table 5-17) to program one statement at a time. If the instrument responds properly, the problem is not hardware related. Troubleshooting assistance may be obtained by calling or writing to the factory (paragraph 5.5.1).

6. Set the RS-232-C configuration DIP switches on the instrument (table 2-4) and terminal for 8 data bits, 1 stop bit, no parity (inhibited). If possible, set the terminal baud rate to 9600 (terminal and instrument baud rates must agree regardless of the value used).
7. Connect a cable between the RS-232-C (DCE) connectors of an ASCII terminal and the unit after verifying cable pins 2 and 3 are **not** reversed between ends.
8. Turn the instrument Power Off for a few seconds, then On to verify power-up reset conditions.
9. Verify proper RS-232-C hardware operation (table 5-17) after noting the following information:
   A) U66 converts a TTL low to +12V, and a TTL high to −12V. U67 converts +12V to a TTL low, and −12V to a TTL high.
   B) Each character entered at the terminal keyboard is immediately transmitted over the RxD line (J3 pin 2), causing U68 pin 30 (INT) to pulse TTL high and U68 pin 14 (CS2) to pulse TTL low. The proper format for the RxD line is a low-to-high transition (start bit) followed by eight data bits (high or low) and one low (stop) bit. Use a scope to monitor the transmission of data over the RxD line by setting the horizontal display for .1 ms (9600 baud), the vertical display for 5 V, and normal trigger mode.
10. If the previous tests have been successful, the problem may be caused by handshaking. Use a full duplex terminal and refer to paragraph 3.4.2.4 for the proper programming sequence.

NOTE

The CD line (J3 pin 8) has not effect on the unit.

Table 5-17. RS-232-C Interface Hardware Checkout

Check	Required Action	Desired Result	Remarks
Enable Active Mode	Bring J3 pin 20 (DTR) high (+12 V) or Send '!' over the RxD line (J3 pin 2)	J3 pin 6 (DSR) goes high (+12 V) and "RS-232 Active" front panel LED becomes lit	Leave active mode enabled
Disable Active Mode	Bring J3 pin 20 (DTR) low (−12 V) or Send '$' over the RxD line (J3 pin 2)	J3 pin 6 (DSR) goes low (−12 V) and "RS-232 Active" front panel LED is extinguished	
Enable Remote Mode	Send 'L0' followed by either <cr> or <lf> over the RxD line (J3 pin 2)	Front panel "Local" LED extinguished and "Remote" LED becomes lit	Leave remote mode enabled
Disable Remote Mode	Send 'L1' followed by either <cr> or <lf> over the RxD line (J3 pin 2)	Front panel "Remote" LED extinguished and "Local" LED becomes lit	
Terminal Controls Instrument	Send 'F1E2S-5I' followed by either <cr> or <lf> over the RxD line (J3 pin 2)	Channel 1 display changes to "−5 dBV FULL SCALE", ".10 kHz CUTOFF FREQ"	
Instrument Data Transmission	Send 'T3', then either <cr> or <lf>, followed by '?' over the RxD line (J3 pin 2)	Terminal displays "C1 F100 S-05 O00 D C2 F10000 S-00 O00 D M000 H0 T3 L0 C1" from the TxD line (J3 pin 3)	

5.5.4.7 IEEE-488 Interface

Related information in this manual.
Schematic: Model 552A; 0103-00-2364 Sheet 4.
Model 553A; 0103-00-2872 Sheet 4.
Circuit Description: Paragraph 4.2.6.

To troubleshoot the IEEE-488 circuitry, do the following:

1. Check +5 V (power supply) at U65 pin 1. If not normal, refer to paragraph 5.5.4.12.
2. Verify a 1.024 MHz clock (50% duty cycle) at U63 pin 6 (CLK).
3. Verify TTL high with 0.5 μs wide TTL low pulses at U82 pin 1.
4. Verify TTL high at U63 pin 40 ($\overline{\text{IRQIEEE}}$).
5. Verify TTL high with negative pulses at U63 pin 3 ($\overline{\text{CS}}$).
6. Verify DIP switches (S1) and pull-up resistors U84) are working properly.
7. Set the instrument rear panel DIP switches for Address 2 and Listen Always disabled (paragraph 2.3.3.2).

NOTE

The remaining steps relate to programming the instrument. Because remote problems are often caused by improper programming format, the user is instructed (table 5-18) to program one statement at a time. If the instrument responds properly, the problem is not hardware related. Although statements in this table were written for the Wavetek Model 6000 Instrumentation Computer, they may be modified to match any GPIB compatible terminal by consulting the instruction manual. Troubleshooting assistance may be obtained by calling or writing to the factory (paragraph 5.5.1).

8. Connect a cable between the IEEE STD 488 connectors of a GPIB compatible terminal and the instrument. Verify no other instruments are connected to the bus.
9. Turn the instrument Power Off for a few seconds, then On to verify power-up reset conditions.

10. Verify proper IEEE-488 hardware operation (table 5-18) after noting the following information:

    A) U64 and U65 are bidirectional transceivers controlled by U63 pins 27 and 28. When the instrument is in listen mode, pins 27 and 28 are low. DAV, NDAC, NRFD, EOI and all eight data lines are driven by the terminal. However, in talk mode, pins 27 and 28 are high, allowing DAV, NDAC, NRFD, EOI and all eight data lines to be driven by the instrument. IFC, ATN and REN are always driven by the terminal and SRQ is always driven by the instrument.

    B) Statements entered at the terminal keyboard are immediately transmitted over the eight data lines (D101 through D108) after pressing the RETURN <ret> or EXECUTE key. U63 pin 40 ($\overline{\text{IRQIEEE}}$) pulses TTL low and U63 pin 3 ($\overline{\text{CS}}$) goes TTL high while data is being transmitted.

Table 5-18. IEEE-488 Interface Hardware Checkout

Check	Program at Terminal	Desired Result	Remarks
Enable Active and Listen Modes	WRITE @702 <ret>	Front Panel GPIB "Active" and "Listen" LED's lit	This addresses the instrument (address "2")
Commands are executed	WRITE @702:"F1E2S-5I" <ret>	Channel 1 display changes to " – 5 dBV FULL SCALE", ".10 kHz CUTOFF FREQ"	
Enable Talk Mode	WRITE @702:"T3" <ret>	No observable change	Enables Talk Mode "3"
	Run the program: 10 DIM A$*60 20 READ @702:A$ 30 END	"Listen" LED extinguished, "Talk" LED lit	Line 10 = Reserve a 60 character DIMension in address A$ Line 20 = Put T3 data in A$
	PRINT A$	Terminal displays "C1 F100 S-05 O00 D C2 F10000 S-00 O00 D M000 H0 T3 L1 C1"	PRINT the contents of A$ on the screen
Accepts Addressed and Universal Keyboard Lockout Commands	WRITE @702:"LO" <ret>	"Local" and "Talk" LEDs extinguished, "Remote" and "Listen" LED's lit	See table 3-2
	WRITE @702:"L1" <ret>	"Remote" LED extinguished, "Local" LED lit	
	LLO @7 <ret>	"Listen" and "Local" LED's extinguished, "Remote" LED lit	See paragraph 3.4.1.3, Universal Commands number 4
	LCL @7 <ret>	"Active" and "Remote" LED's extinguished, "Local" LED lit	

5.5.4.8 Amplifier/Attenuator

Related information in this manual.

Schematic: Model 552A; 0103-00-2364 Sheet 1.
Model 553A; 0103-00-2872 Sheet 1.

Circuit Description: Paragraph 4.2.1.

To troubleshoot the Amplifier/Attenuator circuit, do the following:

1. Program the instrument for a failed condition.
2. Verify source voltages (tables 5-19 and 5-20). If not normal, refer to paragraph 5.5.4.12.
3. Verify U6 and U7 (U30 and U31) pin 2 is approximately +1.3V.
4. Verify 0.5 ms negative going pulse at U8 (U32) pin 11 and U9 (U33) pin 9 each time AC/DC Coupling button pressed.
5. Use tables 5-21, 5-22 and 5-23 to check the On/Off status of relays and FET's for the programmed FULL SCALE and AC/DC settings.
6. One or more FULL SCALE settings shown in table 5-24 should cause the problem to appear. Select the appropriate setting, inject the required signal at Input 1 (Input 2) and verify the test points.
7. Do calibration procedure (paragraph 5.4).

Table 5-19. Source Voltages Originating From +V0

Source Point	Approximate Difference From +V0
+V1 (+V7)	−1.5V
+V2 (+V8)	−0.3V
+V3 (+V9)	−0.7V

Table 5-20. Source Voltages Originating From −V0

Source Point	Approximate Difference From −V0
−V1 (−V7)	+1.4V
−V2 (−V8)	+0.3V
−V3 (−V9)	+0.5V

Table 5-21. Relay and FET Status for Selected FULL SCALE Sensitivity

	FULL SCALE Sensitivity (dB)																
	+dB					−dB											
Relay/FET	20	15	10	5	0	5	10	15	20	25	30	35	40	45	50	55	60
K2 (K16)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1
K3 (K17)	0	0	0	0	1	1	1	1	0	0	0	0	0	0	0	0	0
K4 (K18)	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0
Q3 (Q53)	1	1	0	0	1	1	0	0	1	1	0	0	0	0	0	0	0
Q4 (Q54)	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0
Q5 (Q55)	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	1
Q6 (Q56)	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
Q8 (Q58)	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0
Q9 (Q59)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1

NOTES

1. "0" indicates that relay or FET is Off.
2. "1" indicates that relay or FET is On.

Table 5-22. Status of Relay Driver U1 (U25)

Relay	Relay Status	7406 Input (Pins 1, 3, 5 and 9)	7406 Output (Pins 2, 4, 6 and 8)
K1 (K15) through K4 (K18)	On	TTL High*	TTL Low
	Off	TTL Low*	TTL High

* If input pins to U1 (U25) are not correct, problem is U9 (U33) or Digital Control (paragraph 5.5.4.1).

Table 5-23. Status of FET Drivers U6/U7 (U30/U31)

FET	FET Status	U6/U7 (U30/U31) Input (Pins 3, 5, 10 and 12)	U6/U7 (U30/U31) Output (Pins 1, 7, 8 and 14)
Q3 (Q53) through Q9 (Q59)	On	TTL High*	+13V
	Off	TTL Low*	−13V

* If input pins to U6 and U7 (U30 and U31) are not correct, problem is U8 (U32), Digital Control (paragraph 5.5.4.1) or Amplifier/Filter Control section (paragraph 5.5.4.2).

Table 5-24. Analog Signal Voltages in Amplifier/Attenuator Circuit

Injected Signal* Amplitude	0 dBV	0 dBV	−35 dBV	−45 dBV
FULL SCALE Setting	+20	−5	−40	−50
Test Point	**Desired Result (Vp-p)**			
TP1 (TP6)	0.2	2.0	0.4	0.14
TP2 (TP7)	0.2	2.0	4.0	0.4
U5 (U29) pin 2	0.12	2.0	2.5	0.25
TP3 (TP8)	0.12	2.0	2.5	2.25
E1 (E8)	0.06	0.9	1.0	1.0

* Inject a 2 kHz sine wave at the amplitude shown for each FULL SCALE Setting.

5.5.4.9 Filter

Related information in this manual.

Schematic: Model 552A; 0103-00-2364 Sheet 2 (3).
Model 553A; 0103-00-2872 Sheet 2 (3).

Circuit Description: Paragraph 4.2.3.

To troubleshoot the Filter circuit, do the following:

1. Verify U13 (U36) and U14 (U37) are pressed firmly into their sockets.
2. Program the instrument for a failed condition.
3. Verify source voltages (tables 5-25 and 5-26). If not normal, refer to paragraph 5.5.4.12.
4. Verify U21 and U22 (U43 and U44) pin 2 is approximately +1.3V.
5. Verify 0.5 ms negative going pulse at U23 (U42) pin 11 and U24 (U41) pin 9 each time a cursor arrow is pressed with CUTOFF FREQuency selected.
6. Use tables 5-27, 5-28, 5-29 and 5-30 to check the On/Off status of relays, FET's and their drivers for the programmed CUTOFF FREQuency and 10 dB Output Gain settings.
7. One or more CUTOFF FREQuency settings shown in table 5-31 should cause the problem to appear. Select the appropriate setting, inject a 500 Hz (15 kHz for high pass filter), 0 dBV sine wave at Input 1 (Input 2) and verify the test points.
8. Do calibration procedure (paragraph 5.4).

Table 5-25. Source Voltages Originating From +V0

Source Point	Approximate Difference From +V0
+V4 (+V10)	−0.2V
+V5 (+V11)	−1.2V
+V6 (+V12)	−1.5V

Table 5-26. Source Voltages Originating From −V0

Source Point	Approximate Difference From −V0
−V4 (−V10)	+0.2V
−V5 (−V11)	+0.8V
−V6 (−V12)	+1.1V

Table 5-27. Relays Enabled for Each Cutoff Frequency

Programmed Cutoff Freq	Relays Enabled*		
	First Stage	Second Stage	Third Stage
10 Hz to 990 Hz	K5 (K19)	K8 (K22)	K11 (K25)
1 kHz to 9.9 kHz	K6 (K20)	K9 (K23)	K12 (K26)
10 kHz to 50 kHz	K7 (K21)	K10 (K24)	K13 (K27)

* Identify the relays enabled in each stage by selecting the appropriate "Programmed Cutoff Frequency" row.

Example: Programmed cutoff frequency = 70 Hz;
Enabled third stage relay = K11 (K25).

Table 5-28. FETs Enabled for Each Cutoff Frequency

Programmed Cutoff Frequency			FETs Enabled*				
10 Hz to 990 Hz	1 kHz to 9.9 kHz	10 kHz to 50 kHz	First Stage	Second Stage		Third Stage	
10	100	1,000	Q17 (Q68)	Q25 (Q76)	Q33 (Q84)	Q41 (Q92)	Q49 (Q100)
20	200	2,000	Q16 (Q67)	Q24 (Q75)	Q32 (Q83)	Q40 (Q91)	Q48 (Q99)

Table 5-28. FETs Enabled for Each Cutoff Frequency (Continued)

Programmed Cutoff Frequency			FETs Enabled*				
10 Hz to 990 Hz	1 kHz to 9.9 kHz	10 kHz to 50 kHz	First Stage	Second Stage		Third Stage	
40	400	4,000	Q15 (Q66)	Q23 (Q74)	Q31 (Q82)	Q39 (Q90)	Q47 (Q98)
80	800	8,000	Q14 (Q65)	Q22 (Q73)	Q30 (Q81)	Q38 (Q89)	Q46 (Q97)
100	1000	10,000	Q13 (Q64)	Q21 (Q72)	Q29 (Q80)	Q37 (Q88)	Q45 (Q96)
200	2000	20,000	Q12 (Q63)	Q20 (Q71)	Q28 (Q79)	Q36 (Q87)	Q44 (Q95)
400	4000	40,000	Q11 (Q62)	Q19 (Q70)	Q27 (Q78)	Q35 (Q86)	Q43 (Q94)
800	8000		Q10 (Q61)	Q18 (Q69)	Q26 (Q77)	Q34 (Q85)	Q42 (Q93)

* To identify the FETs enabled for each stage, do the following:

1. Select the "Programmed Cutoff Frequency" column covering the programmed frequency.
2. Select the numeric values listed in that column that, when added together, total the programmed frequency.
3. The enabled FETs for each stage are found in the respective row.

Example: Programmed cutoff frequency = 70 Hz;
Enabled FETs (third stage) = Q39 (Q90), Q40 (Q91), Q41 (Q92), Q47 (Q98), Q48 (Q99) and Q49 (Q100).

Table 5-29. Status of Relay Driver U20 (U39)

Relay	Relay Status	75494 Input (Pins 2, 5, 7, and 10)	75494 Output (Pins 3, 4, 6, and 11)
K5 (K19) through K14 (K28)	On	TTL High*	TTL Low
	Off	TTL Low*	TTL High

* If input pins to U20 (U39) are not correct, problem is U24 (U41), sip U28 (U40) or Digital Control (paragraph 5.5.4.1).

Table 5-30. Status of FET Drivers U21/U22 (U43/U44)

FET	FET Status	U21/U22 (U43/U44) Input (Pins 3, 5, 10 and 12)	U21/U22 (U43/U44) Output (Pins 1, 7, 8 and 14)
Q10 (Q61) through Q49 (Q100)	On	TTL High*	+13V
	Off	TTL Low*	−13V

* If input pins to U21 and U22 (U43 and U44) are not correct, problem is U23 (U42), Digital Control (paragraph 5.5.4.1) or Amplifier/Filter Control section (paragraph 5.5.4.2).

Table 5-31. Analog Signal Voltages in Filter Circuit

CUTOFF FREQuency Setting	660 Hz	990 Hz	10 kHz
Test Point	**Desired Result (Vp-p)**		
U12 (U35) pin 3	0.3	0.4	0.5
E6 (E13)	0.3	0.4	0.6
U13 (U36) pin 1	0.32	0.125	Negligible
U13 (U36) pin 2	0.04	0.04	Negligible
U13 (U36) pin 3	0.04	0.04	Negligible
U13 (U36) pin 6	Virtual Ground		
TP4 (TP5)	0.45	0.25	0.03
U13 (U36) pin 9	Virtual Ground		
U13 (U36) pin 8	0.6	0.5	0.6
U13 (U36) pin 13	Virtual Ground		
E7 (E14)	1.2	1.1	1.3
U14 (U37) pin 1	1.4	0.6	Negligible
U14 (U37) pin 2	0.4	0.275	0.04
U14 (U37) pin 3	0.4	0.275	0.04
U14 (U36) pin 6	Virtual Ground		
U14 (U37) pin 7	1.4	0.9	0.9
U14 (U37) pin 8	1.3	1.3	1.3
U14 (U36) pin 9	Virtual Ground		
U14 (U36) pin 13	Virtual Ground		
U14 (U37) pin 14	1.3	1.3	1.3

5.5.4.10 Output Amplifier

Related information in this manual.
Schematic: Model 552A; 0103-00-2364 Sheet 2 (3).
Model 553A; 0103-00-2872 Sheet 2 (3).
Circuit Description: Paragraph 4.2.3.

Output Amplifier U19 (U38) has a gain of 10 dB and follows switchable 10 dB attenuator R105 (R217).

To troubleshoot the Output Amplifier circuit, do the following:

1. Program the instrument for a failed condition.
2. Verify +V6 (+V12) and −V6 (−V12) source voltages (table 5-32). If not normal, refer to paragraph 5.5.4.12.
3. Verify 0.5 ms negative going pulse at U24 (U41) pin 9 each time the Output Gain button is pressed.
4. Use table 5-33 to check the On/Off status of relay K14 (K28) and Relay Driver U20 (U39) for the programmed 10 dB Output Gain setting.
5. Program the instrument for 0 dBV FULL SCALE and a CUTOFF FREQuency of 10 kHz (400 Hz for high pass filter). Inject a 2 kHz, 0 dBV sine wave at Input 1 (Input 2), then use table 5-34 to check the output amplifier circuit voltages and troubleshoot accordingly.
6. Do calibration procedure (paragraph 5.4).

Table 5-32. Source Voltages +V6 (+V12) and −V6 (+V12)

Source Point	Approximate Difference From V0
+V6 (+V12)	−1.5V from +V0
−V6 (−V12)	+1.1V from −V0

Table 5-33. Status of K14 (K38) and Relay Driver U20 (U39)

	U20 (U39) Pin 10	U20 (U39) Pin 11
Output Gain Off (Relay K14 On)	TTL High*	TTL Low
Output Gain On (Relay K14 Off)	TTL Low*	TTL High

* If U20 (U39) pin 10 is not correct, problem is U24 (U41), sip U28 (U40) or Digital Control (paragraph 5.5.4.1).

Table 5-34. Output Amplifier Circuit Voltages

Test Point	Desired Result (Vp-p)	
	10 dB Output Gain Off	10 dB Output Gain On
U19 (U38) pin 2	0.4	1.3
U19 (U38) pin 3	0.4	1.3
U19 (U38) pin 6	1.3	4.0

5.5.4.11 Overload Circuit

Related information in this manual.

Schematic: Model 552A; 0103-00-2364 Sheet 2 (3).
Model 553A; 0103-00-2872 Sheet 2 (3).
Circuit Description: Paragraph 4.2.2.

When the overload circuit is working normally, a signal causing the voltage at U10 (U34) pins 7 or 8 to be outside the boundaries set by U10 (U34) pins 4 (approximately +0.67) and 6 (approximately -0.67) will cause an overload.

To troubleshoot the Overload circuit, do the following:

1. Verify +V0 (0.1 V below +15 V supply) and −V0 (0.1 V above −15 V supply) voltages. If not normal, refer to paragraph 5.5.4.12.
2. Verify U10 (U34) pin 4 is approximately +0.67 V.
3. Verify U10 (U34) pin 6 is approximately −0.67 V.
4. Program the instrument for 0 dBV FULL SCALE and a CUTOFF FREQuency of 10 kHz. Inject a 2 kHz, 0 dBV sine wave at Input 1 (Input 2), then use table 5-35 to check the overload circuit voltages and troubleshoot accordingly.

Table 5-35. Overload Circuit Voltages

Test Point	Normal Operation	Overload Condition**
U10 (U34) pin 1	+15V	−15V
U10 (U34) pin 2	+14.5V	−9.1V
U10 (U34) pin 11	+14.9V	−15V
U10 (U34) pin 5*	+13.5V	−14.2V
U71 (U70) pin 2	+14.5V	−9.0V
U71 (U70) pin 4	+0.7V	+5.0V

* Use a X10 probe to measure U10 (U34) pin 5.
** To obtain an "Overload Condition" for this test, increase the signal amplitude at AMP 1 to slightly outside the boundaries set by U10 (U34) pins 4 and 6.

5.5.4.12 Power Supply

Use table 5-36 to troubleshoot the power supplies.

Table 5-36. Power Supply Troubleshooting

Problem	Possible Cause	Action
Wrong or no voltage output: (+15 and −15 V supplies)	Wrong line voltage	Check line voltage selector in fuse holder
	Blown fuse	Check fuse
Wrong or no voltage output: (+15 or −15 V supplies)	Bad supply	Return to factory*
	Supply loaded by short on board	Trace to short; look for hot component
No +5 V at U8, U23, U32 or U42	Bad regulator	Verify VR1 input (+15 V supply) and output (+5 V)
	Bad +15V or −15V supply	Return to factory*

*See paragraph 5.5.1.

5.5.4.13 ±12V DC Supply

Related information in this manual.

Schematic: Model 552A; 0103-00-2364 Sheet 5.
Model 553A; 0103-00-2872 Sheet 5.
Circuit Description: Paragraph 4.2.8.

Use table 5-37 to troubleshoot the ±12V DC Supply.

Table 5-37. ±12V DC Supply Voltages

Test Point	Desired Result
Q101 Base	+4 V dc with peaks reaching +5 V
Q102 Base	+0.75 to -4.0V, 50% duty cycle square wave
Q103 Base	+0.8 to 0 V, 60% positive duty cycle square wave
Q103 Collector	+12.5 to 0 V, 40% positive duty cycle square wave
CR118 Cathode	−12.0 to +0.5 V, 40% positive duty cycle square wave

5.5.5 TROUBLESHOOTING INDIVIDUAL COMPONENTS

5.5.5.1 Transistor

1. A transistor is defective if more than 1Vdc is measured across its base-emitter junction in the forward direction.
2. A transistor, when used as a switch, may have a few volts reverse bias voltage across the base-emitter junction.
3. If the collector and emitter voltages are the same, but the base-emitter voltage is less than 500 mV forward voltage or reversed bias, the transistor is defective.
4. In a transistor differential pair (common emitter stages), either their base voltages are the same in normal operating condition, or the one with less forward voltage across its base-emitter junction should be off (no collector current); otherwise one of the transistors is defective.

5.5.5.2 Diode

1. A diode (except a zener) is defective if there is greater than 1Vdc (typically 0.7Vdc) forward voltage across it.

5.5.5.3 Operational Amplifier

1. Generally the "+" and "−" inputs of an operational amplifier will have less than 15 mV difference when operating under normal conditions.
2. When the output of the amplifier is connected to the "−" input (voltage follower connection), the output should be the same voltage as the "+" input voltage; otherwise, the operational amplifier is defective.
3. If the output voltage stays at maximum positive, the "+" input voltage should be more positive than "−" input voltage, or vice versa; otherwise, the operational amplifier is defective.

5.5.5.4 FET Transistor

1. No measurable gate current should be drawn by either gate of U2 (U26). If so, the transistor is defective. Gate-to-source voltage of U2 (U26) is always reverse biased under normal operating conditions.
2. All FET's used as switches in this instrument work identically. For the FET to be On, the cathode of the control diode is brought to near +15V, allowing the gate to float to the drain potential. All three FET pins are at the same potential and the FET conducts. For the FET to be Off, the cathode of the control diode is brought to near −15V, pulling the gate negative with respect to the drain. The source floats to the same potential as the end of the source resistor that is away from the FET.

5.5.5.5 Capacitor

1. Shorted capacitors have 0V across their terminals.
2. Open capacitors can often be located by using a good capacitor connected in parallel with the capacitor under test and observing the resulting effect.
3. Leaky capacitors will often have a decreased voltage across their terminals.

SECTION 6
PARTS AND SCHEMATICS

6.1 DRAWINGS

The following assembly drawings (with parts lists) and schematics are in the arrangement shown below.

6.2 ADDENDA

Under Wavetek's product improvement program, the latest electronic designs and circuits are incorporated into each Wavetek instrument as quickly as development and testing permit. Because of the time needed to compose and print instruction manuals, it is not always possible to include the most recent changes in the initial printing. Whenever this occurs, addendum pages are prepared to summarize the changes made and are inserted immediately inside the rear cover. If no such pages exist, the manual is correct as printed.

6.3 ORDERING PARTS

When ordering spare parts, please specify part number, next higher assembly, and serial number of the instrument.

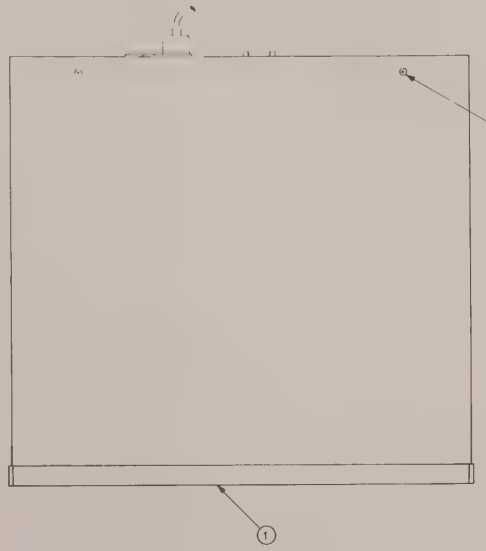
NOTE

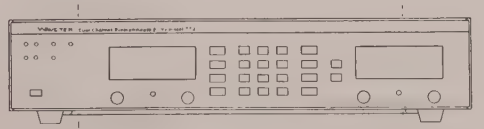
The number etched into a PC board is the bare board part number. The assembly (board and components on the board) part number is stamped on the board. The assembly drawing number is not necessarily the assembly number. However, the assembly number and the parts list number are always the same.

DRAWING		DRAWING NUMBER
Main Assembly	Model 552A	1000-00-0433
	Model 553A	1000-00-0493
Main Assembly Parts List	Model 552A	1000-00-0433
	Model 553A	1000-00-0493
Main Chassis-Sub Assembly	Model 552A	1101-00-2360
	Model 553A	1101-00-2871
Chassis-Sub Assembly Parts List	Model 552A	1101-00-2360
	Model 553A	1101-00-2871
Front Panel Schematic	Models 552A/553A	0103-00-2365
Front Panel PCA	Models 552A/553A	1100-00-2365
Front Panel PCA Parts List	Models 552A/553A	1100-00-2365
Front Panel Assembly	Model 552A	1206-00-2362
	Model 553A	1206-00-2873
Front Panel Parts List	Model 552A	1206-00-2362
	Model 553A	1206-00-2873
Rear Panel Schematic	Models 552A/553A	0103-00-2363
Rear Panel Assembly	Models 552A/553A	1206-00-2363
Rear Panel Parts List	Models 552A/553A	1206-00-2363
Mainboard Schematic	Model 552A	0103-00-2364
	Model 553A	0103-00-2872
Mainboard Assembly	Model 552A	1100-00-2364
	Model 553A	1100-00-2872
Mainboard Parts List	Model 552A	1100-00-2364
	Model 553A	1100-00-2872

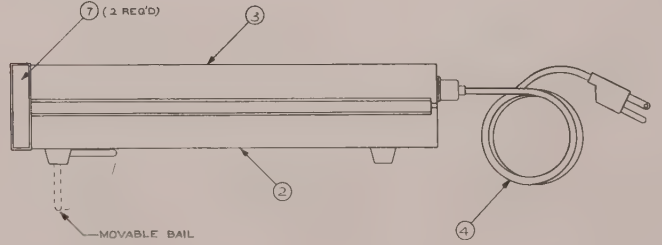
THIS DOCUMENT CONTAINS PROPRIETARY INFORMATION AND DESIGN RIGHTS BELONGING TO WAVETEK AND MAY NOT BE REPRODUCED WITHOUT WRITTEN AUTHORIZATION FOR ANY REASON EXCEPT CALIBRATION OPERATION AND MAINTENANCE

ZONE	LTR	ECO NO	CHANGED BY	APPR'D BY	DATE
	A	RELEASE			10/21/93
	B	3693	N P 11/6/95		11/6/95





NOTE:
ITEM 5 INSTRUCTION MANUAL

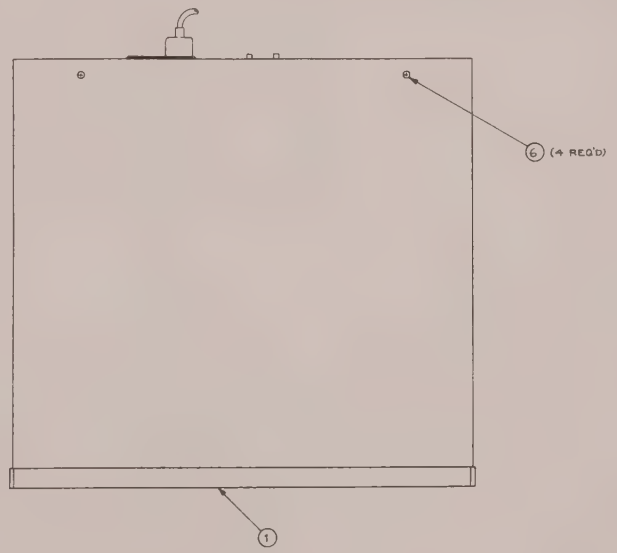


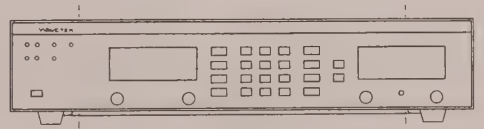
SHEET 2 OF 2 IS "A" SIZE L/M

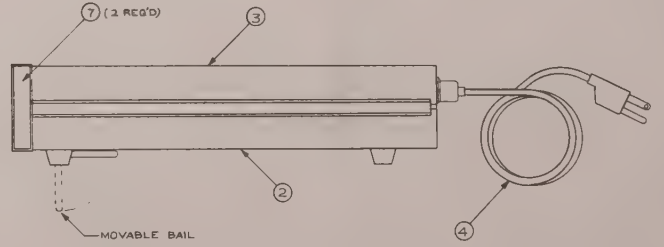
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND TOLERANCES ARE	DO NOT SCALE DWG REMOVE ALL BURRS BREAK SHARP EDGES	WAVETEK Wavetek Inc.	
XX ± 1/64 | XXX ± .005 | XX ± .01 | ± 1°	DRAWN	DATE 10/21/93	TITLE MAIN ASSY 2 CHANNEL FILTER
MATERIAL	CHKD		
FINISH	ENG APPR		
	MFG APPR		SIZE D | MODEL NO 552 | DRAWING NO 1000-00-0433 | REV B
	ISSUED		SCALE 1:2 | CODE IDENT 23338 | SHEET 1 OF 2

THIS DOCUMENT CONTAINS PROPRIETARY IN FORMATION AND DESIGN RIGHTS BELONGING TO WAVETEK AND MAY NOT BE REPRODUCED WITHOUT WRITTEN AUTHORIZATION FOR ANY REASON EXCEPT CALIBRATION OPERATION AND MAINTENANCE

ZONE	LTR	ECO NO	CHANGED BY	APPR'D BY	DATE
	A	RELEASE			







NOTE:
ITEM 5 INSTRUCTION MANUAL

SHEET 2 OF 2 IS "A" SIZE L/M

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND TOLERANCES ARE: X/64 ± 1/64, XXX ± .005, XX ± .01, ∠ ± 1°	DO NOT SCALE DWG REMOVE ALL BURRS BREAK SHARP EDGES	WAVETEK Wavetek Inc.
MATERIAL	DRAWN P. Pitts DATE 3-7-84	TITLE MAIN ASSY 2 CHANNEL FILTER
FINISH	CHKD	
	ENG APPR	
	MFG APPR	
	ISSUED	SIZE D · MODEL NO 554 · DRAWING NO [illegible] · REV A
		SCALE 1:2 · CODE IDENT NO 23338 · SHEET 1 OF 2

THIS DOCUMENT CONTAINS PROPRIETARY INFORMATION AND DESIGN RIGHTS BELONGING TO WAVETEK AND MAY NOT BE REPRODUCED FOR ANY REASON EXCEPT CALIBRATION OPERATION, AND MAINTENANCE WITHOUT WRITTEN AUTHORIZATION

REV	ECN	BY	DATE	APP

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
NONE	MAIN CHASSIS SUB ASSY	552-2360	WVTK	1101-00-2360	1
NONE	COVER ASSY, BOTTOM	552-2339	WVTK	1206-00-2339	1
NONE	INSTRUCTION MANUAL MODEL 552	1300-00-0433	WVTK	1300-00-0433	1
NONE	DECAL, DRESS	604-7920	WVTK	1400-01-7920	2
NONE	COVER, TOP	552-0182	WVTK	1400-02-0182	1
NONE	SCREW, FH, 100 DEG BLK OX, 6-32 X 1/4	6-32 X 1/4 FH, 100	CMRCL	2900-43-6104	4
NONE	PWR CORD 3 COND IEC, USA	17230	BELDN	378, 4007	1

WAVETEK PARTS LIST	TITLE	ASSEMBLY NO.	REV
	FILTER, TWO CHANNEL, MAIN ASSY MODEL 552	1000-00-0433	B
		PAGE 1	

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
NONE	CHASSIS, MAIN	1101-00-2871	WVTK	1101-00-2871	1
NONE	COVER ASSY, BOTTOM	552-2339	WVTK	1206-00-2339	1
NONE	INSTRUCTION MANUAL MODEL 552	1300-00-0433	WVTK	1300-00-0433	1
NONE	DECAL, DRESS	604-7920	WVTK	1400-01-7920	2
NONE	COVER, TOP	552-0182	WVTK	1400-02-0182	1
NONE	SCREW, FH, 100 DEG BLK OX, 6-32 X 1/4	6-32 X 1/4 FH, 100	CMRCL	2900-43-6104	4
NONE	PWR CORD 3 COND IEC, USA	17230	BELDN	378, 4007	1

WAVETEK PARTS LIST	TITLE	ASSEMBLY NO.	REV
	MODEL 553	1000-00-0493	A
		PAGE 1	

WAVETEK SAN DIEGO, CALIFORNIA

TITLE	MODEL NO.	DWG NO.	REV
PARTS LIST MAIN ASSEMBLY	552A	1000-00-0433	B
	553A	1000-00-0493	A
	CODE IDENT 23338	SHEET 1 OF 1	

NOTE UNLESS OTHERWISE SPECIFIED

B-SIZE GRAPHICS/ACCUPRESS REORDER NO. A-0001

REV	ECN	BY	DATE	APP

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
NONE	MAIN CHASSIS SUB ASSY	552-2360	WVTK	1101-00-2360	1
NONE	COVER ASSY, BOTTOM	552-2359	WVTK	1206-00-2359	1
NONE	INSTRUCTION MANUAL MODEL 552	1300-00-0433	WVTK	1300-00-0433	1
NONE	DECAL, DRESS	604-7920	WVTK	1400-01-7920	2
NONE	COVER, TOP	552-0182	WVTK	1400-02-0182	1
NONE	SCREW, FH, 100 DEG BLK OX, 6-32 X 1/4	6-32 X 1/4 FH, 100	CMCL	2800-43-6104	4
NONE	PWR CORD: 3 COND IEC, USA	17230	BELDN	378.4007	1

WAVETEK PARTS LIST

TITLE: FILTER, TWO CHANNEL MAIN ASSY MODEL 552

ASSEMBLY NO. 1000-00-0433 REV B

PAGE 1

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO	QTY/PT
NONE	CHASSIS, MAIN SUB-ASSY	1101-00-2871	WVTK	1101-00-2871	1
NONE	COVER ASSY, BOTTOM	552-2359	WVTK	1206-00-2359	1
NONE	INSTRUCTION MANUAL MODEL 552	1300-00-0433	WVTK	1300-00-0433	1
NONE	DECAL, DRESS	604-7920	WVTK	1400-01-7920	2
NONE	COVER, TOP	552-0182	WVTK	1400-02-0182	1
NONE	SCREW, FH, 100 DEG BLK OX, 6-32 X 1/4	6-32 X 1/4 FH, 100	CMCL	2800-43-6104	4
NONE	PWR CORD: 3 COND IEC, 6834	17230	BELDN	378.4007	1

WAVETEK PARTS LIST

TITLE: MODEL 553

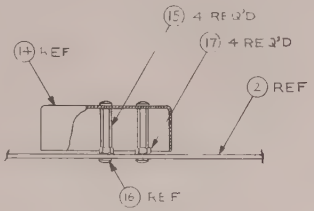
ASSEMBLY NO. 1000-00-0493 REV A

PAGE 1

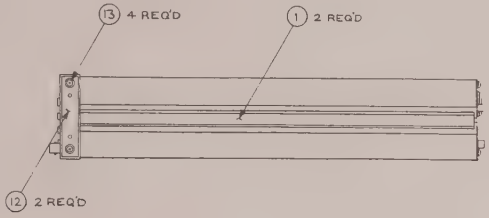
WAVETEK SAN DIEGO, CALIFORNIA

TITLE	MODEL NO	DWG NO	REV
PARTS LIST MAIN ASSEMBLY	552A	1000-00-0433	B
	MODEL NO 553A	DWG NO 1000-00-0493	REV A
	CODE IDENT 23338	SHEET 1 OF 1	

ZONE	LTR	ECO NO	CHANGED BY	APPR'D BY	DATE
	A	RELEASE			
	B	[illegible]	01 12 93 RD	[illegible]	[illegible]



SECTION A-A
(SCALE 1:1)



SHEET 2 OF 2 IS "A" SIZE L/M

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND TOLERANCES ARE	DO NOT SCALE DWG REMOVE ALL BURRS BREAK SHARP EDGES	WAVETEK Wavetek Inc.
x/x ± 1/64 · xxx ± .005 · xx ± .01 · ± 1°	DRAWN [illegible] DATE 8/4/86	TITLE
MATERIAL:	CHKD	MAIN CHASSIS-SUB ASSEMBLY
FINISH	ENG APPR	
	MFG APPR	SIZE D · MODEL NO 55 · DRAWING NO 1101-00-2811 · REV B
	SCALE 1/2 · FSCM NO/DWG NO 23338	SHEET 1 OF 2

THIS DOCUMENT CONTAINS PROPRIETARY INFORMATION AND DESIGN RIGHTS BELONGING TO WAVETEK AND MAY NOT BE REPRODUCED FOR ANY REASON EXCEPT CALIBRATION OPERATION AND MAINTENANCE WITHOUT WRITTEN AUTHORIZATION

REV	ECN	BY	DATE	APP

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO	QTY/PT
NONE	ASSY, MAIN BOARD	552-2364	WVTK	1100-00-2364	1
NONE	FRONT PANEL MODEL 552	552-2362	WVTK	1206-00-2362	1
NONE	PANEL ASSY, REAR	552-2363	WVTK	1206-00-2363	1
NONE	SOCKET: 34PIN DIL LOCK CLSEND	3414-7034	3M	353 3402	1
NONE	CABLE 34CND COL/RIB 28GA .050			378 4020	1
NONE	FRONT VERTICAL TRIM CAP	604-7841	WVTK	1400-01-7841	2
NONE	INSERT, SIDE PANEL	552-0710	WVTK	1400-02-0710	2
NONE	SHIELD: DRAWN CAN	1400-02-2309	WVTK	1400-02-2309	2
NONE	FLAT CABLE CLIP	FCA-15	MEXBR	2800-00-0027	2
NONE	SCREW, SELF TAPPING TYPE B, PAN CROSS	8-18 X 1/2	CMRCL	2800-22-8208	4
NONE	SCREW, PAN CAD I, CROSS RECESS,	MS51957-15	COML	2800-38-4106	4
NONE	M SCR, ST CD PH 4-40 X 1/4 PH			381 4042	16
NONE	MSCR SS PHLPS 6X32X3/8 100FH	6X32X3/8 100FH	CMRCL	385 6064	4

WAVETEK PARTS LIST	TITLE: MAIN CHASSIS SUB ASSY	ASSEMBLY NO: 1101-00-2360	REV: D

PAGE 1

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO	QTY/PT
NONE	NUT HX ST CD 4-40 X 3/16AF			387 4060	8
NONE	NUT, HEX SS 6-32 X 1/4AF			387.6081	2
NONE	WASHER EXT LK STL CAD 86			388 1061	2
NONE	SPR THD 3/16HX 4-40X3/4	1656A	KEYST	389 2005	8
NONE	GUIDE PIN ASSY FEM METRIC	552633-3	AMP	389.7004	1

WAVETEK PARTS LIST	TITLE: MAIN CHASSIS SUB ASSY	ASSEMBLY NO: 1101-00-2360	REV: D

PAGE 2

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO	QTY/PT
NONE	PCA, MAINBOARD 553	1100-00-2872	WVTK	1100-00-2872	1
NONE	PANEL ASSY, REAR	552-2363	WVTK	1206-00-2363	1
NONE	PANEL ASSY, FRONT-553	1206-00-2873	WVTK	1206-00-2873	1
NONE	SOCKET 34PIN DIL LOCK CLSEND	3414-7034	3M	353 3402	1
NONE	CABLE 34CND COL/RIB 28GA .050			378 4020	1
NONE	FRONT VERTICAL TRIM CAP	604-7841	WVTK	1400-01-7841	2
NONE	INSERT, SIDE PANEL	552-0710	WVTK	1400-02-0710	2
NONE	SHIELD DRAWN CAN	1400-02-2309	WVTK	1400-02-2309	2
NONE	SCREW, SELF TAPPING TYPE B, PAN CROSS	8-18 X 1/2	CMRCL	2800-22-8208	4
NONE	SCREW, PAN CAD I, CROSS RECESS,	MS51957-15	COML	2800-38-4106	4
NONE	NUT HEX SS 6-32 X 1/4AF			387 6081	2
NONE	WASHER EXT LK STL CAD 86			388 1061	2
NONE	GUIDE PIN ASSY FEM METRIC	552633-3	AMP	389 7004	1

WAVETEK PARTS LIST	TITLE: CHASSIS, MAIN SUB-ASSY	ASSEMBLY NO: 1101-00-2871	REV: C

PAGE 1

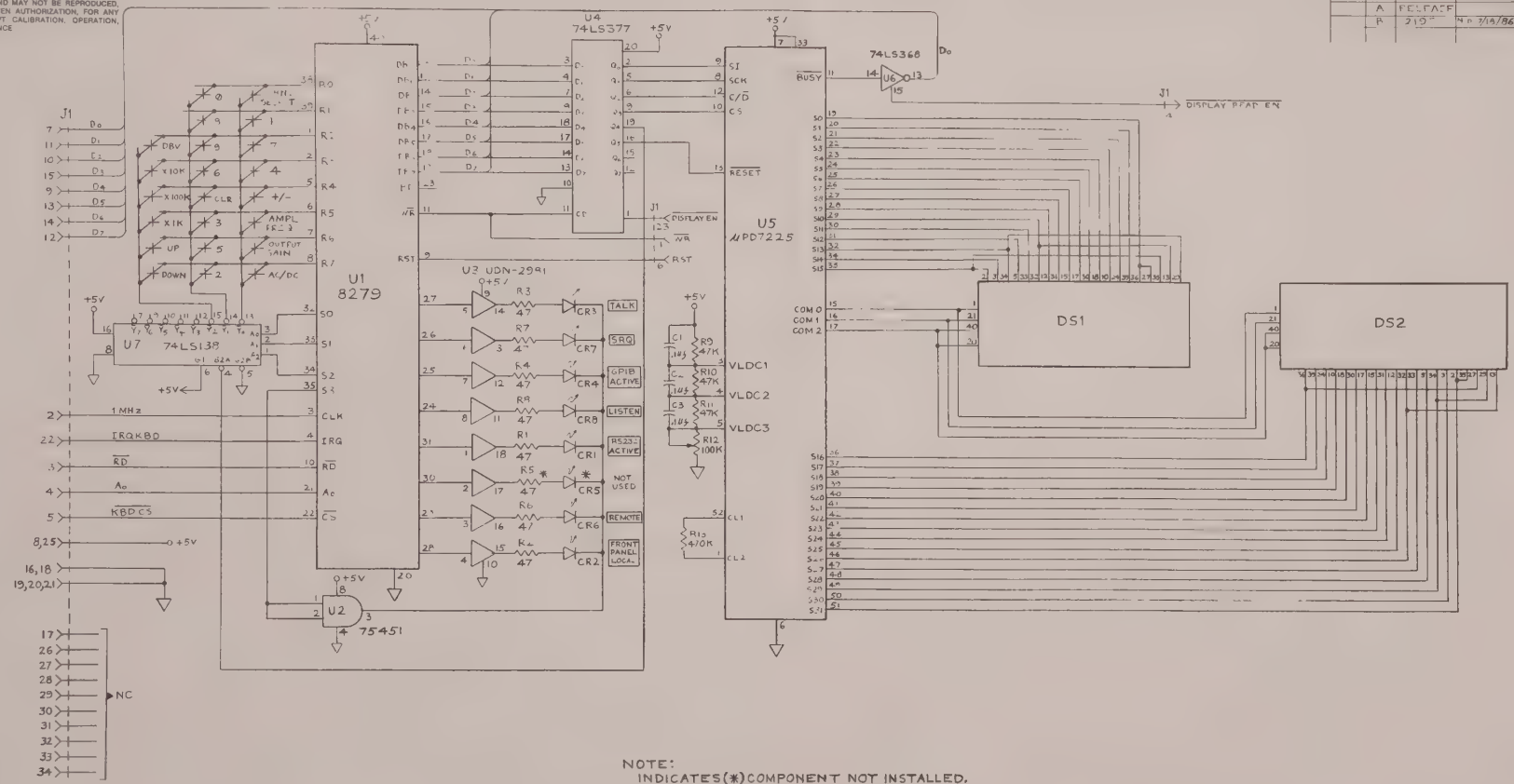
NOTE: UNLESS OTHERWISE SPECIFIED

WAVETEK SAN DIEGO, CALIFORNIA

TITLE	MODEL NO.	DWG NO.	REV
PARTS LIST CHASSIS SUB-ASSEMBLY	552A	1101-00-2360	D
	MODEL NO. 553A	DWG NO. 1101-00-2871	REV C
	CODE IDENT 23338	SHEET 1 OF 1	

THIS DOCUMENT CONTAINS PROPRIETARY INFORMATION AND DESIGN RIGHTS BELONGING TO WAVETEK AND MAY NOT BE REPRODUCED, WITHOUT WRITTEN AUTHORIZATION, FOR ANY REASON EXCEPT CALIBRATION, OPERATION, AND MAINTENANCE

ZONE	LTR	ECO NO	CHANGED BY	APPR'D BY	DATE
	A	RELEASE			3/1/96
	B	219	ND 7/18/96	DMA	7/11/96

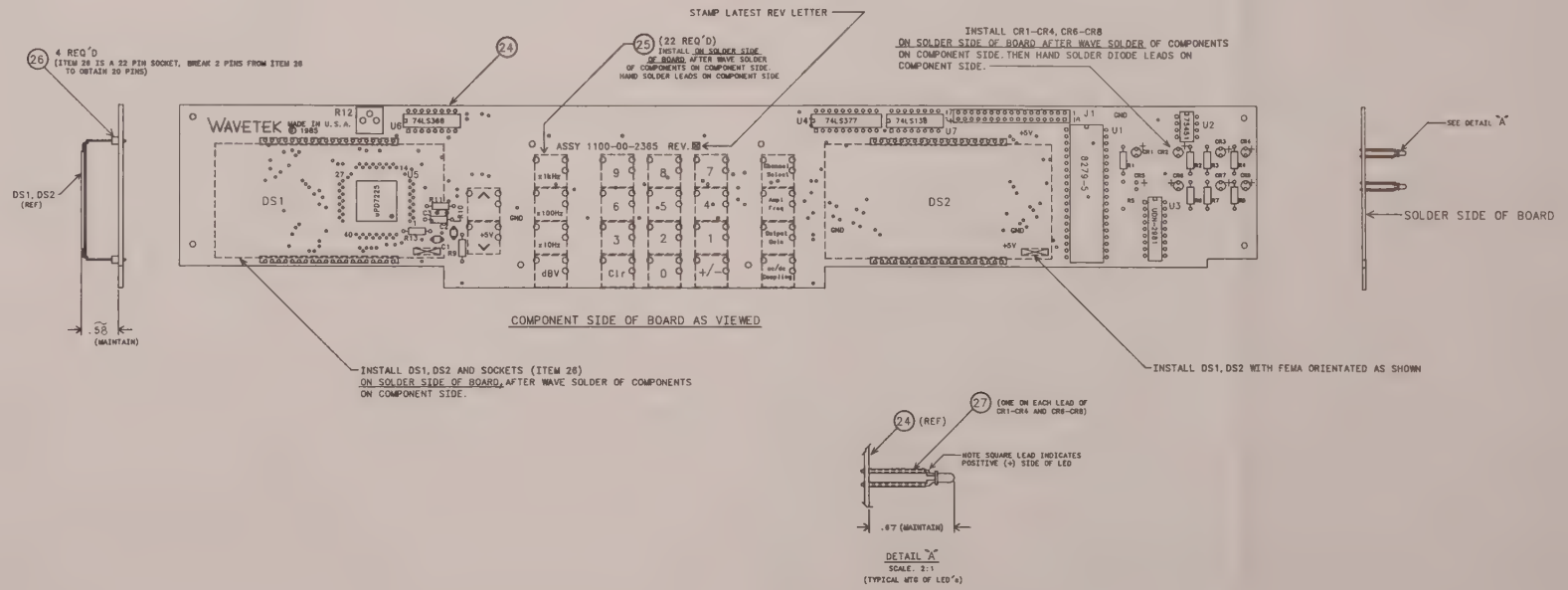


NOTE:
INDICATES(*)COMPONENT NOT INSTALLED.

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND TOLERANCES ARE: .xx ± 1/64, .xxx ± .005, ∠ ± 1°	DO NOT SCALE DWG REMOVE ALL BURRS BREAK SHARP EDGES	WAVETEK
MATERIAL	DRAWN	TITLE: ELECTRICAL SCHEMATIC FRONT PANEL BD.
FINISH	CHKD	
	ENG APPR	
	MFG APPR	
	ISSUED	SIZE: D; MODEL NO: [illegible]; DRAWING NO: [illegible]-00-2365; REV: B
		SCALE: N; CODE IDENT: 23335; SHEET 1 OF 1

THIS DOCUMENT CONTAINS PROPRIETARY INFORMATION AND DESIGN RIGHTS BELONGING TO WAVETEK AND MAY NOT BE REPRODUCED, WITHOUT WRITTEN AUTHORIZATION, FOR ANY REASON EXCEPT CALIBRATION, OPERATION, AND MAINTENANCE.

ZONE	LTR	ECO NO.	CHANGED BY	APPRD BY	DATE
	A	RELEASE		R.H.	11/22/85
	B	ECO 2043	M.P. 11/20/85	R.H.	11/22/85
	C	ECO 2083	M.P. 2/28/86	[illegible]	[illegible]
	D	ECO [illegible]	M.P. 5/2/86	[illegible]	[illegible]
	E	[illegible]	M.P. [illegible]	[illegible]	[illegible]


STAMP LATEST REV LETTER
26 4 REQ'D (ITEM 28 IS A 22 PIN SOCKET, BREAK 2 PINS FROM ITEM 28 TO OBTAIN 20 PINS)
24
25 (22 REQ'D) INSTALL ON SOLDER SIDE OF BOARD AFTER WAVE SOLDER OF COMPONENTS ON COMPONENT SIDE. HAND SOLDER LEADS ON COMPONENT SIDE
INSTALL CR1–CR4, CR6–CR8 ON SOLDER SIDE OF BOARD AFTER WAVE SOLDER OF COMPONENTS ON COMPONENT SIDE. THEN HAND SOLDER DIODE LEADS ON COMPONENT SIDE.
DS1, DS2 (REF)
.58 (MAINTAIN)
WAVETEK MADE IN U.S.A. © 1985
ASSY 1100-00-2365 REV.
DS1
DS2
82726-5
SEE DETAIL 'A'
SOLDER SIDE OF BOARD
COMPONENT SIDE OF BOARD AS VIEWED
INSTALL DS1, DS2 AND SOCKETS (ITEM 28) ON SOLDER SIDE OF BOARD, AFTER WAVE SOLDER OF COMPONENTS ON COMPONENT SIDE.
INSTALL DS1, DS2 WITH FEMA ORIENTATED AS SHOWN
27 (ONE ON EACH LEAD OF CR1–CR4 AND CR6–CR8)
24 (REF)
NOTE SQUARE LEAD INDICATES POSITIVE (+) SIDE OF LED
.87 (MAINTAIN)
DETAIL 'A'
SCALE. 2:1
(TYPICAL MTG OF LED's)

SHEETS 2 OF 2 ARE "A" SIZE L/M's

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND TOLERANCES ARE: X/X ±1/64, .XXX ±.005, .XX ±.01, ∠ ±1°	DO NOT SCALE DWG REMOVE ALL BURRS BREAK SHARP EDGES	WAVETEK Wavetek Inc.	
MATERIAL:	DRAWN N. PETERS 10/16/85	TITLE: P.C. ASSEMBLY FRONT PANEL	
FINISH:	CHKD S.R. 11/22/85		
	ENG APPR. P.M. 11/22/85		
	MFG APPR R.H. 11/22/85		
	ISSUED	SIZE D / MODEL NO 552 / DRAWING NO. 1100-00-2365 / REV E	
		SCALE. 1.25:1 / 23338 / SHEET 1 OF 2	

THIS DOCUMENT CONTAINS PROPRIETARY INFORMATION AND DESIGN RIGHTS BELONGING TO WAVETEK AND MAY NOT BE REPRODUCED FOR ANY REASON EXCEPT CALIBRATION OPERATION AND MAINTENANCE WITHOUT WRITTEN AUTHORIZATION

REV	ECN	BY	DATE	APP

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO	QTY/PT
C1 C2 C3	C FX MONO 0 1UF 50V Z5U	SR215E104ZAT	AVX	100 4102	3
R1 R2 R3 R4 R5 R6 R7 R8	R FX CFLM 47 OHM 5% 1/4W			116 0471	8
R10 R11 R9	R FX CFLM 47K OHM 5% 1/4W			116 3471	3
R13	R FX CFLM 470K OHM 5% 1/4W			116 4471	1
R12	R VAR CMT 100K 3/8SQ	72XR100K	BECK	118 [illegible]	1
U5	SMD. FLATPACK. LCD CONTROLLER/DRIVER	UPD7225G00	NEC	120 4025	1
U3	U LED DRIVER. NON-INV	[illegible]	SPRAG	120 4081	1
U2	U DUAL PRPHL DRIVER (75451)	SN75451BN/P3	TI	120 4451	1
U7	U 3 TO 8 LINE DECOD (74LS138)	74LS138N/AT	NSC	[illegible] 0115	1
U6	U HX BUS DRIV INV 3ST (LS368)	SN74LS368N	TI	125 0132	1
U1	KEYBOARD ENCODER	UPD-8279-5	NEC	129 3204	1
NONE	PCB.DD.FRONT PANEL	1700-00-2365	WVTK	1700-00-2365	1

WAVETEK PARTS LIST | TITLE: ASSY. FRONT PANEL | ASSEMBLY NO: 1100-00-2365 | REV | PAGE 1

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO	QTY/PT
	(552)				
LED1 LED2 LED3 LED4 LED5 LED6 LED7	LED RED. MIN 2MCD@10. 70DVA	HLMP-1301	HP	171 1603	7
J1	CONN TERM 34 PIN DIL [illegible]	929663-01-17	A/P	354 0003	1
NONE	NUT HEX SS 6-32 X 1/4AF			387 6081	8
NONE	WASHER FLAT BTL CAD [illegible]			388 0060	8
LCD1 LCD2	DISPLAY LCD 1 2X3 2 IN CUSTOM	254	FEMA	4899-00-0048	2
U4	TTL D-FF OCT	74LS377	TI	8007-43-7710	1

WAVETEK PARTS LIST | TITLE: ASSY. FRONT PANEL | ASSEMBLY NO: 1100-00-2365 | REV | PAGE 2

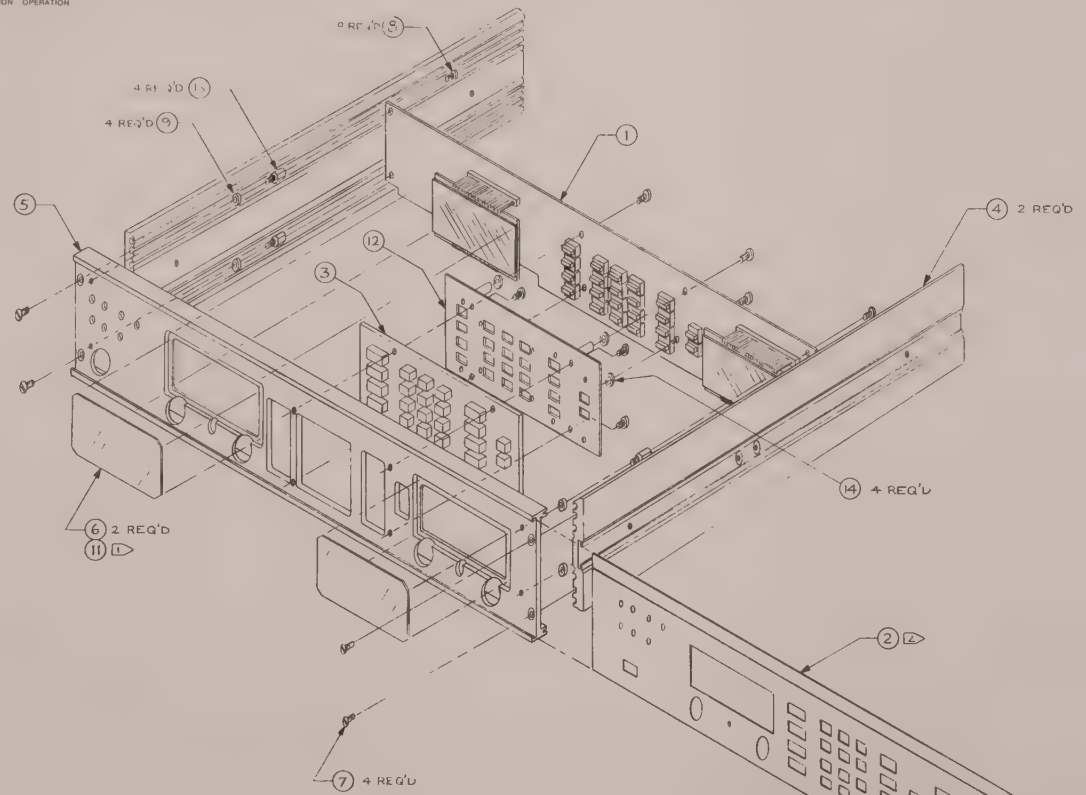
REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN	DATE	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL	PROJENGR		TITLE: PARTS LIST FRONT PANEL PCA
	RELEASE APPROV		
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ± .010 ANGLES ± 1 XX ± .030		
	DO NOT SCALE DWG		DWG NO: 1100-00-2365 REV: E
	SCALE		552A/553A
			CAGE 23338 SHEET 1 OF 1

NOTE UNLESS OTHERWISE SPECIFIED

BISHOP GRAPHICS/ACCUPRESS REORDER NO. X-2894

THIS DOCUMENT CONTAINS PROPRIETARY IN FORMATION AND DESIGN RIGHTS BELONGING TO WAVETEK AND MAY NOT BE REPRODUCED WITHOUT WRITTEN AUTHORIZATION, FOR ANY REASON EXCEPT CALIBRATION OPERATION AND MAINTENANCE

ZONE	LTR	ECO NO	CHANGED BY	APPR'D BY	DATE
	A	RELEASE			7/1/94
	B	1-05	1-28-96		1/4/96



NOTE:

(1) SECURE ITEM 6 TO FRONT OF PANEL BY TACKING FOUR CORNERS WITH ITEM 11.

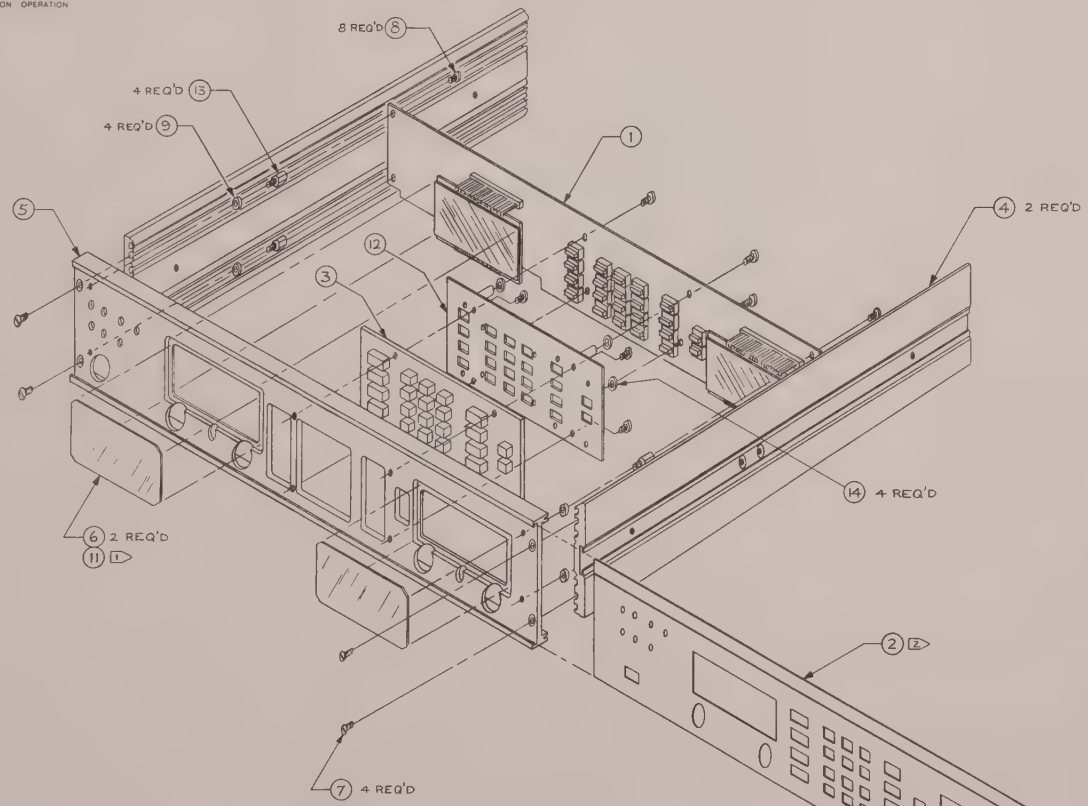
(2) INSERT OVERLAY (ITEM 2) INTO FRONT PANEL (ITEM 5) BEFORE MOUNTING KEYPAD (ITEM 3)

SHEET 2 OF 2 IN "A" SIZE L/M

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND TOLERANCES ARE: x/n ± 1/64, xxx ± .005, xx ± .01, ± 1°	DO NOT SCALE DWG REMOVE ALL BURRS BREAK SHARP EDGES	WAVETEK Wavetek Inc.	
MATERIAL	DRAWN	TITLE: PANEL ASSEMBLY FRONT	
FINISH	CHKD		
	ENG APPR		
	MFG APPR		
	ISSUED	SIZE: D	MODEL NO: 1210
		DRAWING NO: 6-00-23362	REV: B
		SCALE: -	CODE IDENT: 23338
		SHEET 1 OF 2	

THIS DOCUMENT CONTAINS PROPRIETARY IN FORMATION AND DESIGN RIGHTS BELONGING TO WAVETEK AND MAY NOT BE REPRODUCED WITHOUT WRITTEN AUTHORIZATION FOR ANY REASON EXCEPT CALIBRATION OPERATION AND MAINTENANCE

ZONE	LTR	ECO NO	CHANGED BY	APPR'D BY	DATE
	A	RELEASE			



NOTE:

1. SECURE ITEM 6 TO FRONT OF PANEL BY TACKING FOUR CORNERS WITH ITEM 11.
2. INSERT OVERLAY(ITEM 2) INTO FRONT PANEL (ITEM 5) BEFORE MOUNTING KEYPAD (ITEM 3)

SHEET 2 OF 2 IS "A" SIZE L/M

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND TOLERANCES ARE X's ± 1/64 · XXX ± .005 · XX ± .01 · ∠ ± 1° MATERIAL FINISH	DO NOT SCALE DWG REMOVE ALL BURRS BREAK SHARP EDGES DRAWN N. Peter DATE 11/4 CHKD ENG APPR MFG APPR ISSUED	WAVETEK Wavetek Inc. TITLE PANEL ASSEMBLY FRONT SIZE D · MODEL NO 55 · DRAWING NO [illegible] · REV A SCALE — · CODE IDENT 23338 · SHEET 1 OF 2

THIS DOCUMENT CONTAINS PROPRIETARY INFORMATION AND DESIGN RIGHTS BELONGING TO WAVETEK AND MAY NOT BE REPRODUCED FOR ANY REASON, EXCEPT CALIBRATION, OPERATION, AND MAINTENANCE WITHOUT WRITTEN AUTHORIZATION

REV	ECN	BY	DATE	APP

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO	QTY/PT
NONE	ASSY. FRONT PANEL	552-2363	WVTK	1100-00-2363	1
NONE	PANEL, SIDE	552-0202	WVTK	1400-02-0202	2
NONE	PANEL, FRONT	552-0220	WVTK	1400-02-0220	1
NONE	MOLDED KEYPAD, 22 KEYS CUSTOM	552-0230	WVTK	1400-02-0230	1
NONE	OVERLAY PANEL	552-0240	WVTK	1400-02-0240	1
NONE	SHIELD, LCD	552-0720	WVTK	1400-02-0720	2
NONE	PLATE, BACKING	1400-02-1893	WVTK	1400-02-1893	1
NONE	SCREW, SELF TAPPING TYPE B, FLAT HD 82DEG	B-16X1/2 F H	CMRCL	2800-22-8908	4
NONE	M SCR ST CD PHIL 6-32 X 1/4			381 6042	8
NONE	WASHER FLT NYL #6 5/16D 1/8T			388 3061	4
NONE	WASHER FLT NYL #6 1/32THK			388 3062	4
NONE	SPR THD M/F 1/4HX 6-32X3/8			389 2014	4

WAVETEK PARTS LIST

TITLE: FRONT PANEL MODEL 552

ASSEMBLY NO. 1206-00-2362

REV B

PAGE 1

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO	QTY/PT
NONE	ASSY. FRONT PANEL	552-2363	WVTK	1100-00-2363	1
NONE	PANEL, SIDE	552-0202	WVTK	1400-02-0202	2
NONE	PANEL, FRONT	552-0220	WVTK	1400-02-0220	1
NONE	MOLDED KEYPAD, 22 KEYS CUSTOM	552-0230	WVTK	1400-02-0230	1
NONE	SHIELD, LCD	552-0720	WVTK	1400-02-0720	2
NONE	PLATE, BACKING	1400-02-1893	WVTK	1400-02-1893	1
NONE	OVERLAY PANEL-553	1400-02-2200	WVTK	1400-02-2200	1
NONE	SCREW, SELF TAPPING TYPE B, FLAT HD 82DEG	B-16X1/2 F H	CMRCL	2800-22-8908	4
NONE	M SCR ST CD PHIL 6-32 X 1/4			381 6042	8
NONE	WASHER FLT NYL #6 5/16D 1/8T			388 3061	4
NONE	WASHER FLT NYL #6 1/32THK			388 3062	4
NONE	SPR THD M/F 1/4HX 6-32X3/8			389 2014	4

WAVETEK PARTS LIST

TITLE: PANEL ASSY. FRONT-553

ASSEMBLY NO 1206-00-2873

REV A

PAGE 1

NOTE UNLESS OTHERWISE SPECIFIED

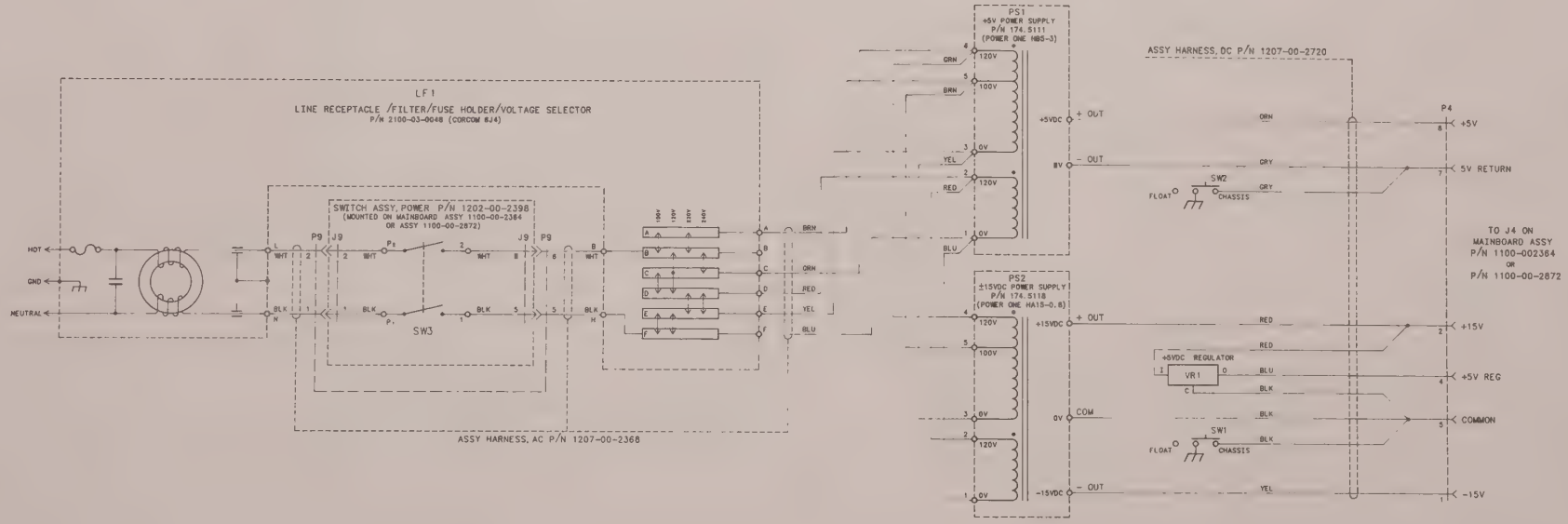
BISHOP GRAPHICS/ACCUPRESS
REORDER NO. A-3884

WAVETEK SAN DIEGO - CALIFORNIA

TITLE	MODEL NO.	DWG NO.	REV
PARTS LIST FRONT PANEL ASSEMBLY	552A	1206-00-2362	B
	MODEL NO. 553A	DWG NO. 1206-00-2873	REV A
	CODE IDENT 23338	SHEET 1 OF 1	

THIS DOCUMENT CONTAINS PROPRIETARY INFORMATION AND DESIGN RIGHTS BELONGING TO WAVETEK AND MAY NOT BE REPRODUCED, WITHOUT WRITTEN AUTHORIZATION. FOR ANY REASON EXCEPT CALIBRATION, OPERATION, AND MAINTENANCE

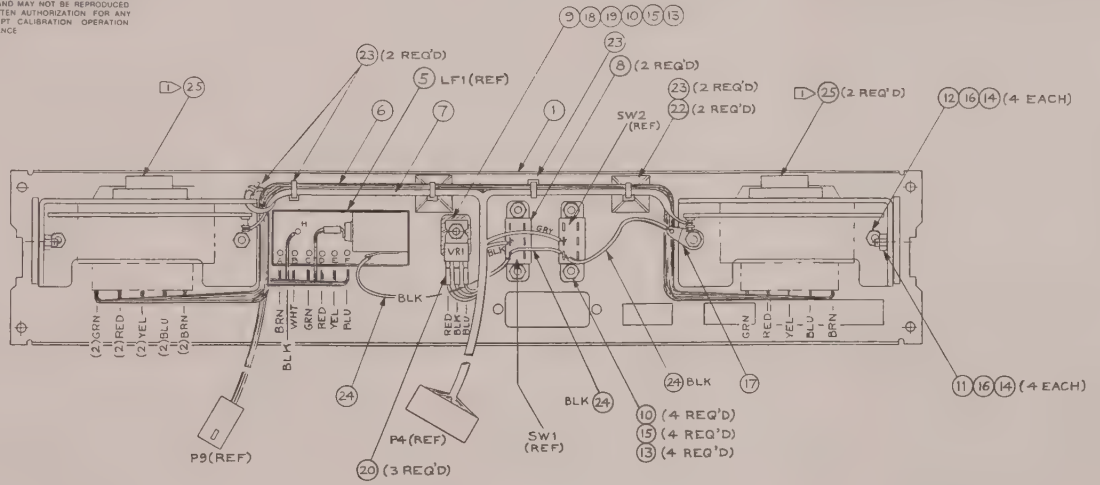
ZONE	LTR	ECO NO	CHANGED BY	APPRD BY	DATE
	A	RELEASE			

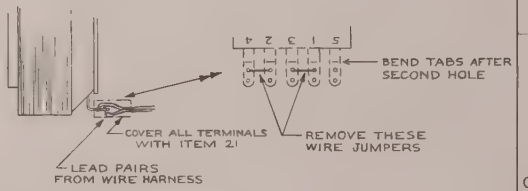


UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND TOLERANCES ARE	DO NOT SCALE DWG REMOVE ALL BURRS BREAK SHARP EDGES	WAVETEK Wavetek Inc.
X/X ±1/64 · XXX ±.005 · XX ±.01 · ±1°	DRAWN PETERS 7/31/86	TITLE: ELECTRICAL SCHEMATIC REAR PANEL
MATERIAL	CHKD	
	ENG APPR	
FINISH	MFG APPR	SIZE D · MODEL NO 552/553 · DRAWING NO -00-2363 · REV A
	ISSUED	SCALE: 23338 · SHEET 1 OF 1

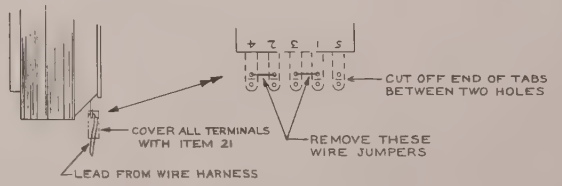
THIS DOCUMENT CONTAINS PROPRIETARY INFORMATION AND DESIGN RIGHTS BELONGING TO WAVETEK AND MAY NOT BE REPRODUCED WITHOUT WRITTEN AUTHORIZATION FOR ANY REASON EXCEPT CALIBRATION OPERATION AND MAINTENANCE

ZONE	LTR	ECO NO	CHANGED BY	APPR'D BY	DATE
	A	RELEASE			
	B	2192	MP 7/15/86		
	C	2227	MP 8/20/86		
A-5	D	7923	MC 1/19/87	RGK	
B-4	E	7942	MC 3/9/87	RGK	

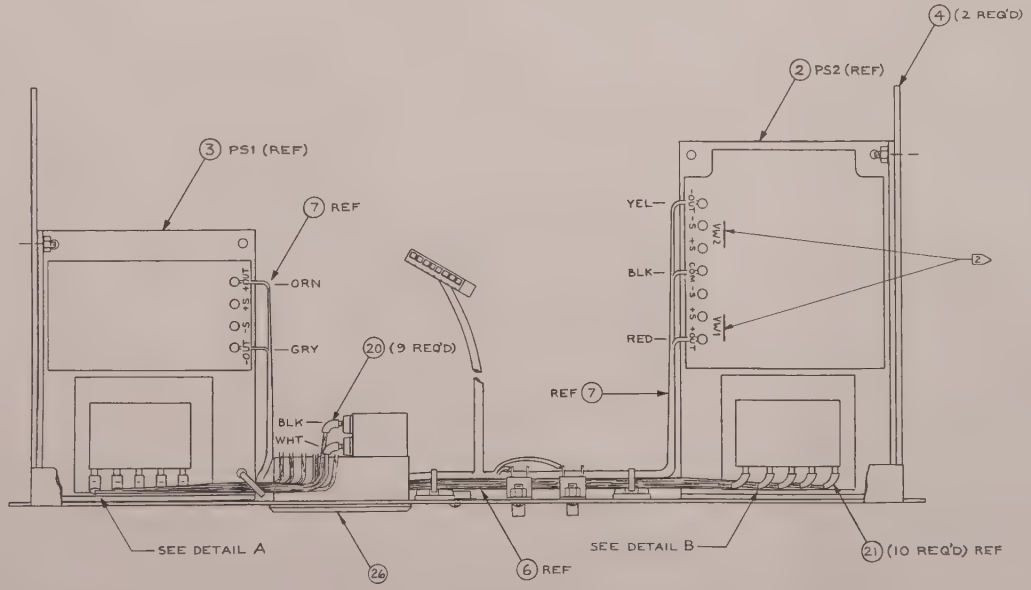




DETAIL A



DETAIL B



NOTE:

1. REMOVE SCREWS FROM POWER TRANSISTORS, COVER TRANSISTORS WITH ITEM 25 & SECURE WITH SAME SCREWS.
2. CUT JUMPERS VW1 AND VW2.

SHEET 2 IS "A" SIZE L/M

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND TOLERANCES ARE: X ± 1/64, XX ± .005, XXX ± .01, ANGLES ± 1°	DO NOT SCALE DWG REMOVE ALL BURRS BREAK SHARP EDGES	WAVETEK Wavetek Inc.	
MATERIAL	DRAWN P. Eckel 11/8/85	TITLE: PANEL ASSY, REAR	
FINISH	CHKD		
	ENG APPR		
	MFG APPR	SIZE: D	MODEL NO: 552/553
	ISSUED	SCALE: 1:1	CODE IDENT: 23338
		DRAWING NO: 1206-00-2363	REV: E
		SHEET 1 OF 2	

THIS DOCUMENT CONTAINS PROPRIETARY INFORMATION AND DESIGN RIGHTS BELONGING TO WAVETEK AND MAY NOT BE REPRODUCED FOR ANY REASON EXCEPT CALIBRATION, OPERATION, AND MAINTENANCE WITHOUT WRITTEN AUTHORIZATION

REV	ECN	BY	DATE	APP

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO	QTY/PT
NONE	5 P.V REG 5V 1A TO 220	LM7805CT	NSC	120 0032	1
NONE	CONN CABLE 6 POS RECP (MOLEX)	03-09-1063	MOLEX	351 0600	1
NONE	CONN TERM PIN .093 (MOLEX)	02-09-2103	MOLEX	354 0013	1
NONE	TIE CABLE NY NAT 3/4 MAX DIA	SST-1-M	PANDT	377 4001	1
NONE	WIRE #22 AWG STR BLACK			378 1604	1
NONE	WIRE #22 AWG STR BRN			378 1614	1
NONE	WIRE #22 AWG STR RED			378 1624	1
NONE	WIRE #22 AWG STR YELLOW			378 1644	1
NONE	WIRE #22 AWG STR GRN			378 1654	1
NONE	WIRE #22 AWG STR BLU			378 1664	1
NONE	WIRE #22 AWG STR WHITE			378 1694	1
NONE	SOCKET HSG BPDS SIL 156 LKG	09-50-3081	MOLEX	353 0804	1
NONE	CONN CRIMP (MOLEX	08-50-0108	MOLEX	354 0012	1

WAVETEK PARTS LIST | TITLE: PANEL ASSY. REAR | ASSEMBLY NO 1206-00-2363 | REV C | PAGE 1

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO	QTY/PT
	KK)				
NONE	TIE CABLE NY NAT 3/4 MAX DIA	SST-1-M	PANDT	377 4001	1
NONE	WIRE #22 AWG STR BLACK			378 1604	1
NONE	WIRE #22 AWG STR RED			378 1624	1
NONE	WIRE #22 AWG STR ORN			378 1634	1
NONE	WIRE #22 AWG STR YELLOW			378 1644	1
NONE	WIRE #22 AWG STR BLU			378 1664	1
NONE	WIRE #22 AWG STR GRY			378 1684	1
NONE	REAR PANEL	552-0250	WVTK	1400-02-0250	1
NONE	PLATE, ADAPTER POWER SUPPLY	552-0263	WVTK	1400-02-0263	2
PS1	POWER SUPPLY 36-03 (A/P)			174 5111	1
PS2	POWER SUPPLY 3 CH SYN. A/P			174 5118	1
NONE	RECEPTACLE	6J4	CORCM	2100-03-0048	1
NONE	S SLIDE DPDT	46206LR	SWCFT	342 2200	2

WAVETEK PARTS LIST | TITLE: PANEL ASSY. REAR | ASSEMBLY NO 1206-00-2363 | REV C | PAGE 2

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO	QTY/PT
NONE	LUG SOLDER FLAT #4LKG 23/32L	1413-4	SMITH	339 0012	1
NONE	CLAMP CABLE TIE	6001-12A	AUGAT	362 1607	2
NONE	COVER TIGTN. NYLON. EYELET TO-3			362 3903	3
NONE	INSULATOR MICA TO-220	4672	KEYST	368 5004	1
MA NONE	TIE CABLE NY NAT 3/4 MAX DIA	SST-1-M	PANDT	377 4001	3
NONE	WIRE #22 AWG STR BLACK			378 1604	5
NONE	SHRINK TBG PLYFIN BLACK 3/16"			378 3530	12
NONE	SHRINK TBG PLYFIN BLACK 3/8"			378 3560	10
NONE	M SCR ST CD PH 4-40 X 3/8 PH			381 4062	5
NONE	M SCR ST CD PHP 6-32 X 1/2 PH			381 6082	4
NONE	M SCR ST N PH 6-32X1/2 100 D FH	6-32X1/2 100 D FH	CMRCL	384 6084	4

WAVETEK PARTS LIST | TITLE: PANEL ASSY. REAR | ASSEMBLY NO 1206-00-2363 | REV C | PAGE 3

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO	QTY/PT
NONE	NUT HEX SS 4-40 X 1/4AF			387 4081	5
NONE	NUT HEX SS 6-32 X 1/4AF			387 6081	8
NONE	WASHER EXT LK STL CAD #4			388 1041	5
NONE	WASHER EXT LK STL CAD #6			388 1061	8
NONE	WASHER PLT NYL #4			388 4040	1

WAVETEK PARTS LIST | TITLE: PANEL ASSY. REAR | ASSEMBLY NO 1206-00-2363 | REV C | PAGE 4

NOTE UNLESS OTHERWISE SPECIFIED

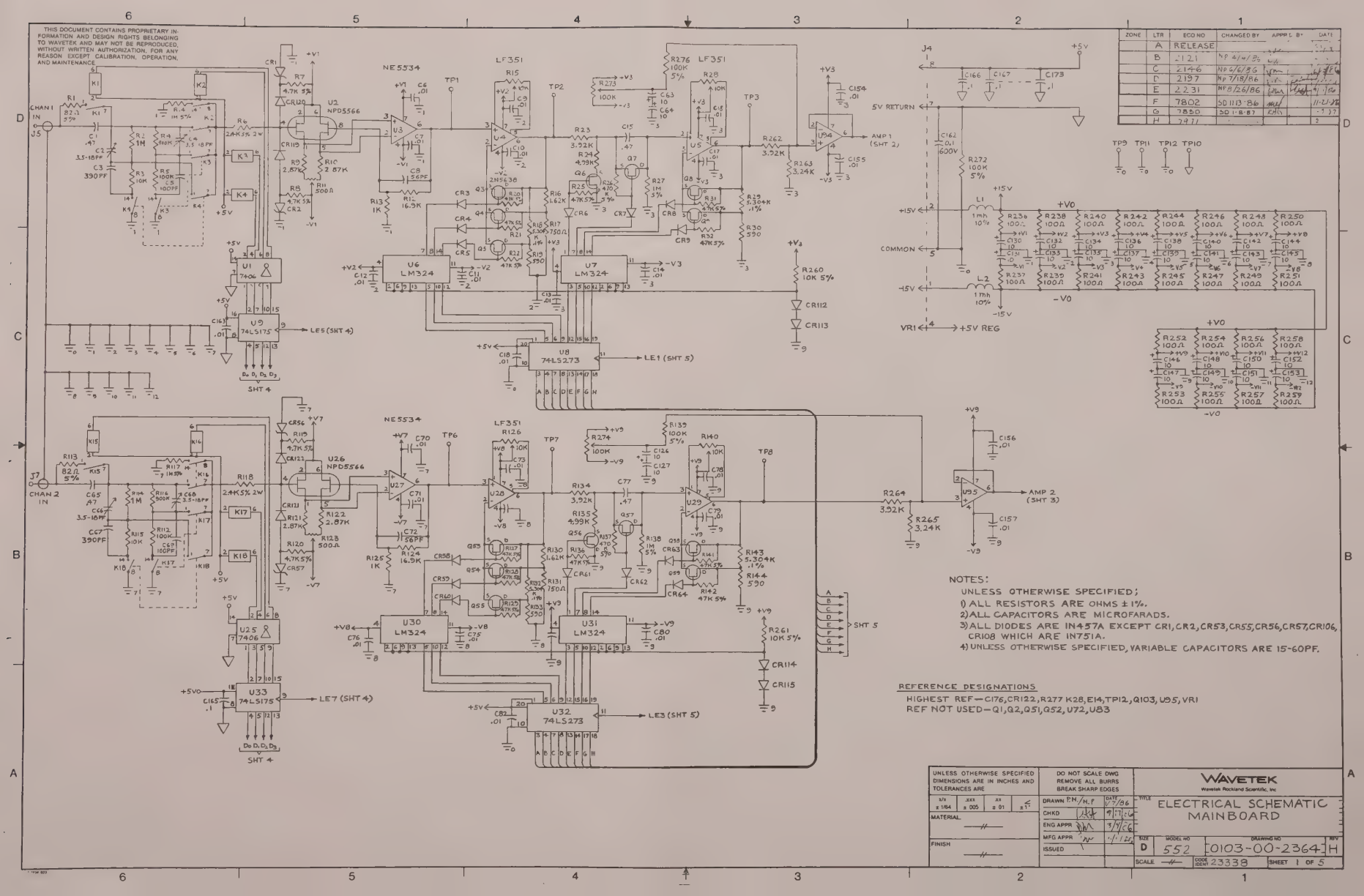
REMOVE ALL BURRS AND BREAK SHARP EDGES | MATERIAL | FINISH WAVETEK PROCESS | DRAWN | DATE | PROJ ENGR | RELEASE APPROV | TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ± .010 ANGLES ±1 XX ± .030 | DO NOT SCALE DWG | SCALE

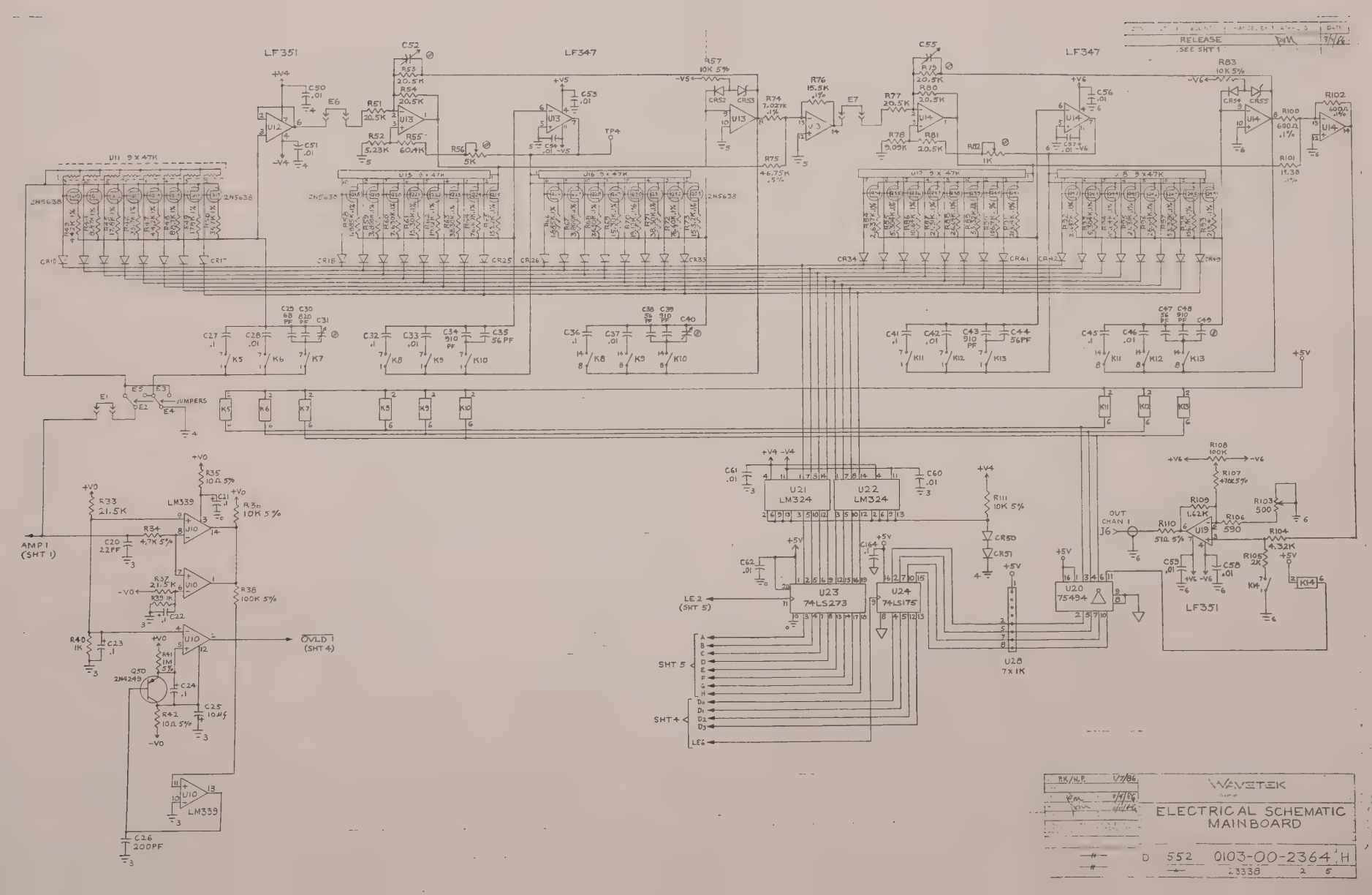
WAVETEK SAN DIEGO, CALIFORNIA

TITLE: PARTS LIST REAR PANEL ASSEMBLY

MODEL NO 552A/553A | DWG NO 1206-00-2363 | REV C | TODAY'S DATE 23338 | SHEET 1 OF 1

BISHOP GRAPHICS, SCOTTSDALE RECORDER NO. N-3884

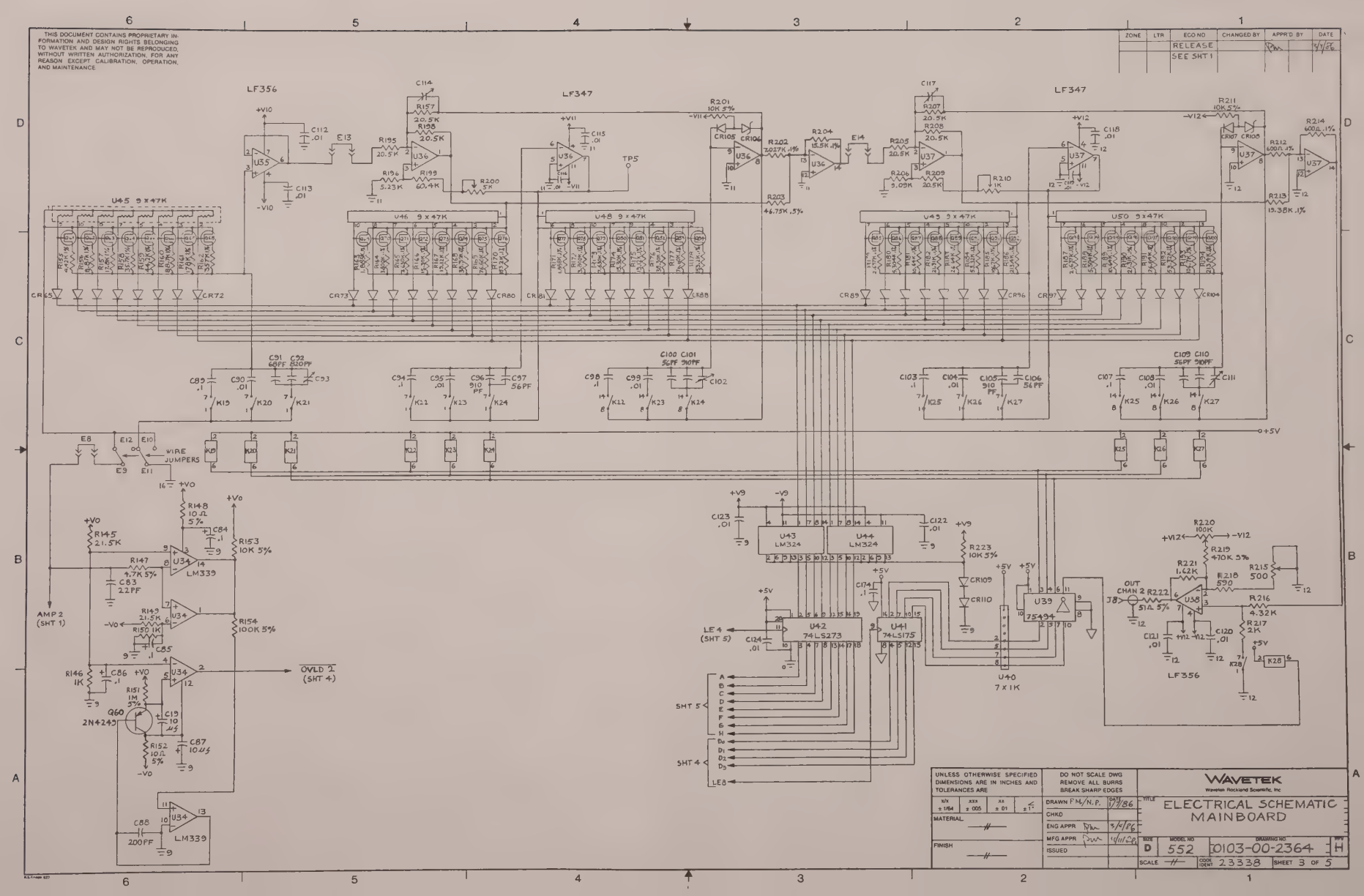

THIS DOCUMENT CONTAINS PROPRIETARY INFORMATION AND DESIGN RIGHTS BELONGING TO WAVETEK AND MAY NOT BE REPRODUCED, WITHOUT WRITTEN AUTHORIZATION, FOR ANY REASON EXCEPT CALIBRATION, OPERATION, AND MAINTENANCE.
ZONE | LTR | ECO NO | CHANGED BY | APPR'L B+ | DATE
A RELEASE
B 2121 NP 4/14/86
C 2146 NP 6/6/86
D 2197 NP 7/18/86
E 2231 NP 8/26/86
F 7802 SD 11-3-86 11-21-86
G 7850 SD 1-8-87
H 7911
CHAN 1 IN
CHAN 2 IN
NE5534
LF351
NPD5566
LM324
74LS175
74LS273
74LS04
74LS06
74LS08
74LS32
74LS74
74LS157
74LS158
74LS174
74LS244
74LS245
74LS373
74LS374
74LS377
74LS393
74LS670
AMP 1 (SHT 2)
AMP 2 (SHT 3)
5V RETURN
+5V REG
COMMON
LE5 (SHT 4)
LE1 (SHT 5)
LE7 (SHT 4)
LE3 (SHT 5)
SHT 4
SHT 5
NOTES:
UNLESS OTHERWISE SPECIFIED;
1) ALL RESISTORS ARE OHMS ± 1%.
2) ALL CAPACITORS ARE MICROFARADS.
3) ALL DIODES ARE IN457A EXCEPT CR1, CR2, CR53, CR55, CR56, CR57, CR106, CR108 WHICH ARE IN751A.
4) UNLESS OTHERWISE SPECIFIED, VARIABLE CAPACITORS ARE 15-60PF.
REFERENCE DESIGNATIONS
HIGHEST REF—C176, CR122, R277 K28, E14, TP12, Q103, U95, VR1
REF NOT USED—Q1, Q2, Q51, Q52, U72, U83
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND TOLERANCES ARE
DO NOT SCALE DWG REMOVE ALL BURRS BREAK SHARP EDGES
MATERIAL
FINISH
DRAWN P.M. 11/1/85
CHKD 9/11/86
ENG APPR 3/1/86
MFG APPR 11/12/86
ISSUED
WAVETEK
Wavetek Rockland Scientific, Inc
TITLE
ELECTRICAL SCHEMATIC
MAINBOARD
SIZE D
MODEL NO 552
DRAWING NO 0103-00-23641
REV H
SCALE
CODE IDENT 23338
SHEET 1 OF 5



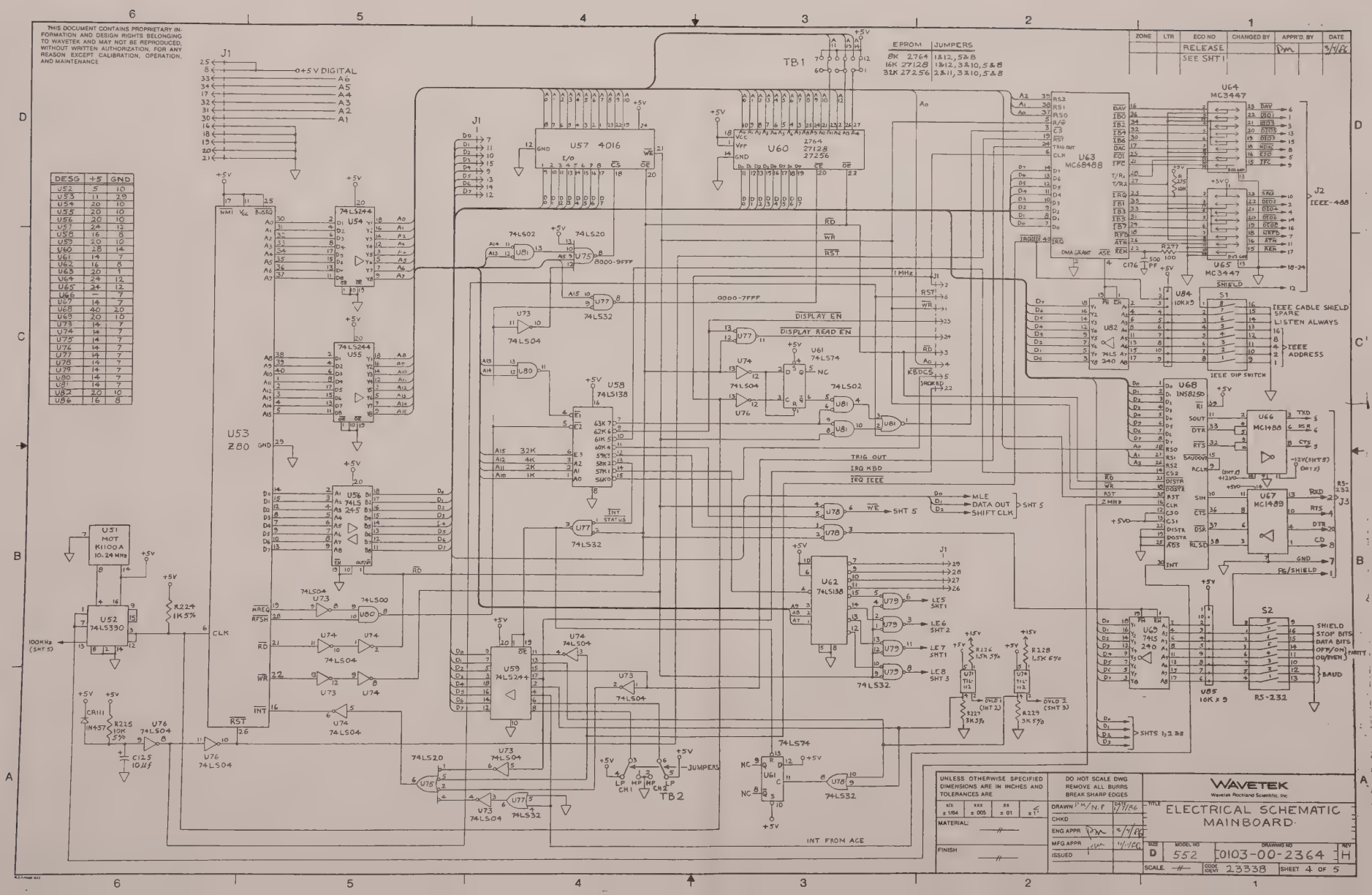
PK/W.P.	7/7/86	WAVETEK
PM	7/7/86	ELECTRICAL SCHEMATIC
		MAINBOARD
#	D 552	0103-00-2364 H
#	23338	2 5

THIS DOCUMENT CONTAINS PROPRIETARY INFORMATION AND DESIGN RIGHTS BELONGING TO WAVETEK AND MAY NOT BE REPRODUCED, WITHOUT WRITTEN AUTHORIZATION. FOR ANY REASON EXCEPT CALIBRATION, OPERATION, AND MAINTENANCE

ZONE	LTR	ECO NO	CHANGED BY	APPR'D BY	DATE
		RELEASE SEE SHT 1			3/4/86

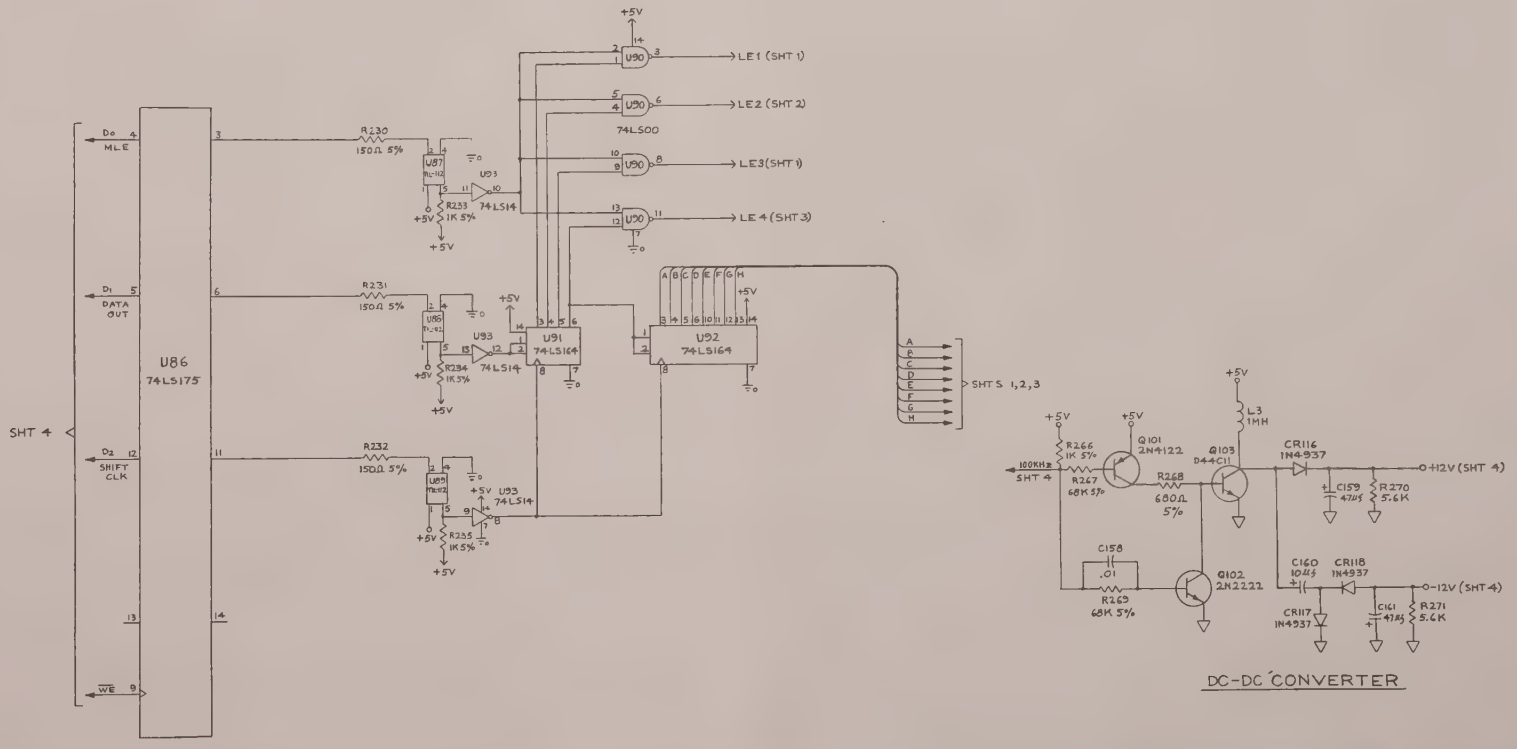


UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND TOLERANCES ARE	DO NOT SCALE DWG REMOVE ALL BURRS BREAK SHARP EDGES	WAVETEK Wavetek Rockland Scientific, Inc
x/x ± 1/64 · xxx ± 005 · xx ± 01 · ∠ ± 1°	DRAWN F.M./N.P. 1/9/86	TITLE ELECTRICAL SCHEMATIC MAINBOARD
MATERIAL —	CHKD	
FINISH —	ENG APPR 3/4/86	
	MFG APPR 1/9/86	SIZE D · MODEL NO 552 · DRAWING NO 0103-00-2364 · REV H
	ISSUED	SCALE — · CODE IDENT 23338 · SHEET 3 OF 5


THIS DOCUMENT CONTAINS PROPRIETARY INFORMATION AND DESIGN RIGHTS BELONGING TO WAVETEK AND MAY NOT BE REPRODUCED, WITHOUT WRITTEN AUTHORIZATION, FOR ANY REASON EXCEPT CALIBRATION, OPERATION, AND MAINTENANCE
ZONE | LTR | ECO NO | CHANGED BY | APPR'D. BY | DATE
RELEASE | | |

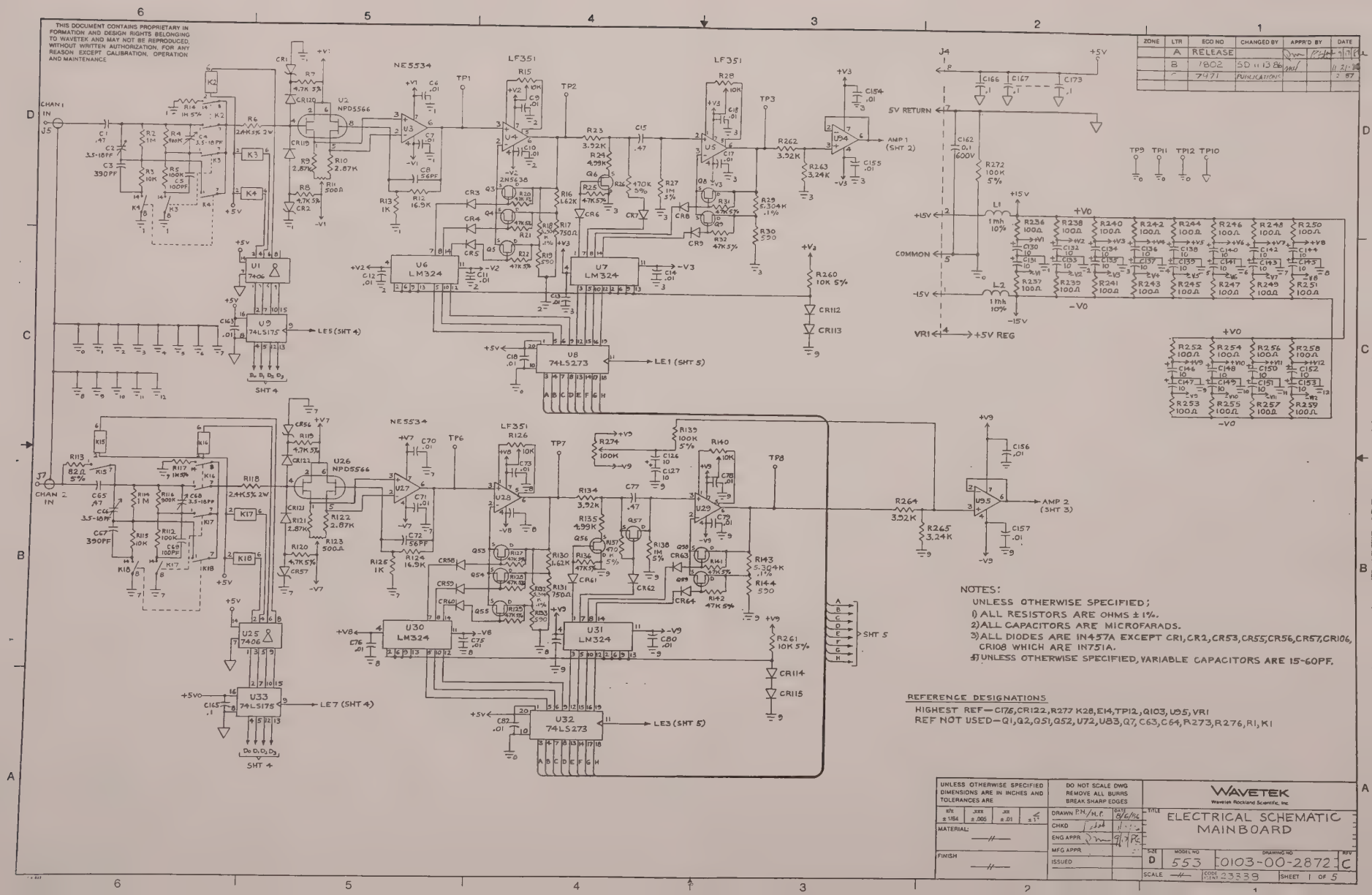
THIS DOCUMENT CONTAINS PROPRIETARY INFORMATION AND DESIGN RIGHTS BELONGING TO WAVETEK AND MAY NOT BE REPRODUCED, WITHOUT WRITTEN AUTHORIZATION, FOR ANY REASON EXCEPT CALIBRATION, OPERATION, AND MAINTENANCE

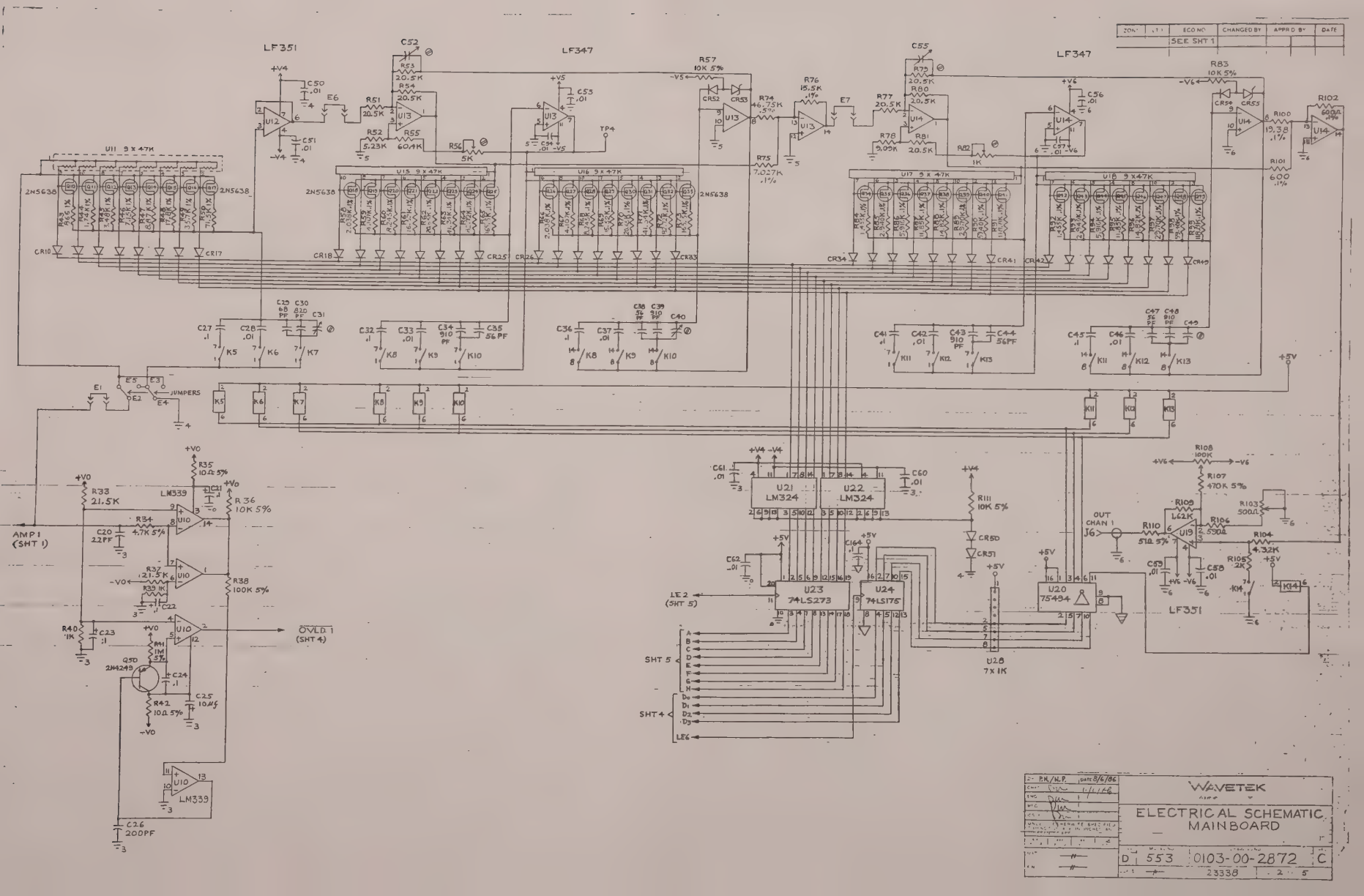
ZONE	LTR	ECO NO	CHANGED BY	APPR'D BY	DATE
		RELEASE SEE SHT 1			7/7/86



DC-DC CONVERTER

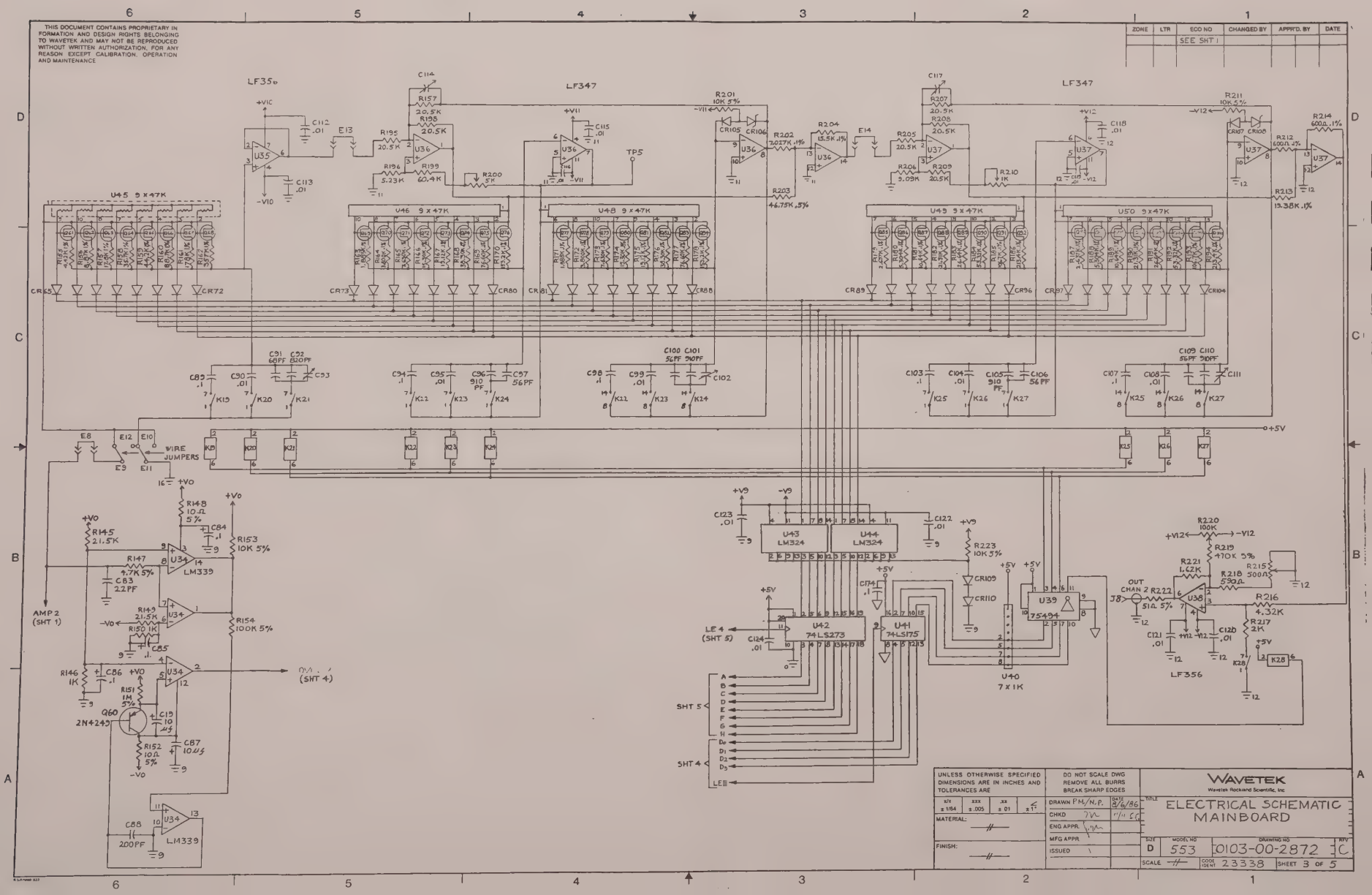
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND TOLERANCES ARE	DO NOT SCALE DWG REMOVE ALL BURRS BREAK SHARP EDGES	WAVETEK Wavetek Rockland Scientific, Inc.
x/x ± 1/64 · xxx ± .005 · xx ± .01 · ± 1°	DRAWN P.M./N.P. DATE 11/1/86	TITLE: ELECTRICAL SCHEMATIC MAINBOARD
MATERIAL —	CHKD	
FINISH —	ENG APPR. DATE 7/7/86	SIZE D · MODEL NO. 552 · DRAWING NO. 0103-00-2364 · REV H
	MFG APPR. DATE 11/11/86	SCALE: — · CODE IDENT 23338 · SHEET 5 OF 5
	ISSUED	


THIS DOCUMENT CONTAINS PROPRIETARY INFORMATION AND DESIGN RIGHTS BELONGING TO WAVETEK AND MAY NOT BE REPRODUCED, WITHOUT WRITTEN AUTHORIZATION, FOR ANY REASON EXCEPT CALIBRATION, OPERATION AND MAINTENANCE
ZONE | LTR | ECO NO | CHANGED BY | APPR'D BY | DATE
A | RELEASE | 9/7/86
B | 7802 | SD | 11/13/86
7471 | PUBLICATIONS | 11/21/86
CHAN 1 IN
CHAN 2 IN
NE5534
LF351
NPD5566
LM324
74LS273
74LS175
74LS175
74LS175
74LS273
5V RETURN
COMMON
+5V REG
AMP 1 (SHT 2)
AMP 2 (SHT 3)
LE5 (SHT 4)
LE1 (SHT 5)
LE7 (SHT 4)
LE3 (SHT 5)
SHT 4
SHT 4
SHT 5
NOTES:
UNLESS OTHERWISE SPECIFIED;
1) ALL RESISTORS ARE OHMS ± 1%.
2) ALL CAPACITORS ARE MICROFARADS.
3) ALL DIODES ARE IN457A EXCEPT CR1, CR2, CR53, CR55, CR56, CR57, CR106, CR108 WHICH ARE IN751A.
4) UNLESS OTHERWISE SPECIFIED, VARIABLE CAPACITORS ARE 15-60PF.
REFERENCE DESIGNATIONS
HIGHEST REF—C176, CR122, R277 K28, E14, TP12, Q103, U35, VR1
REF NOT USED—Q1, Q2, Q51, Q52, U72, U83, Q7, C63, C64, R273, R276, R1, K1
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND TOLERANCES ARE
DO NOT SCALE DWG REMOVE ALL BURRS BREAK SHARP EDGES
MATERIAL:
FINISH
DRAWN P.N./M.P. 9/6/86
CHK'D
ENG APPR 9/7/86
MFG APPR
ISSUED
WAVETEK
Wavetek Rockland Scientific, Inc.
TITLE
ELECTRICAL SCHEMATIC
MAINBOARD
SIZE D
MODEL NO 553
DRAWING NO 0103-00-2872
REV C
SCALE —
CODE IDENT 23339
SHEET 1 OF 5

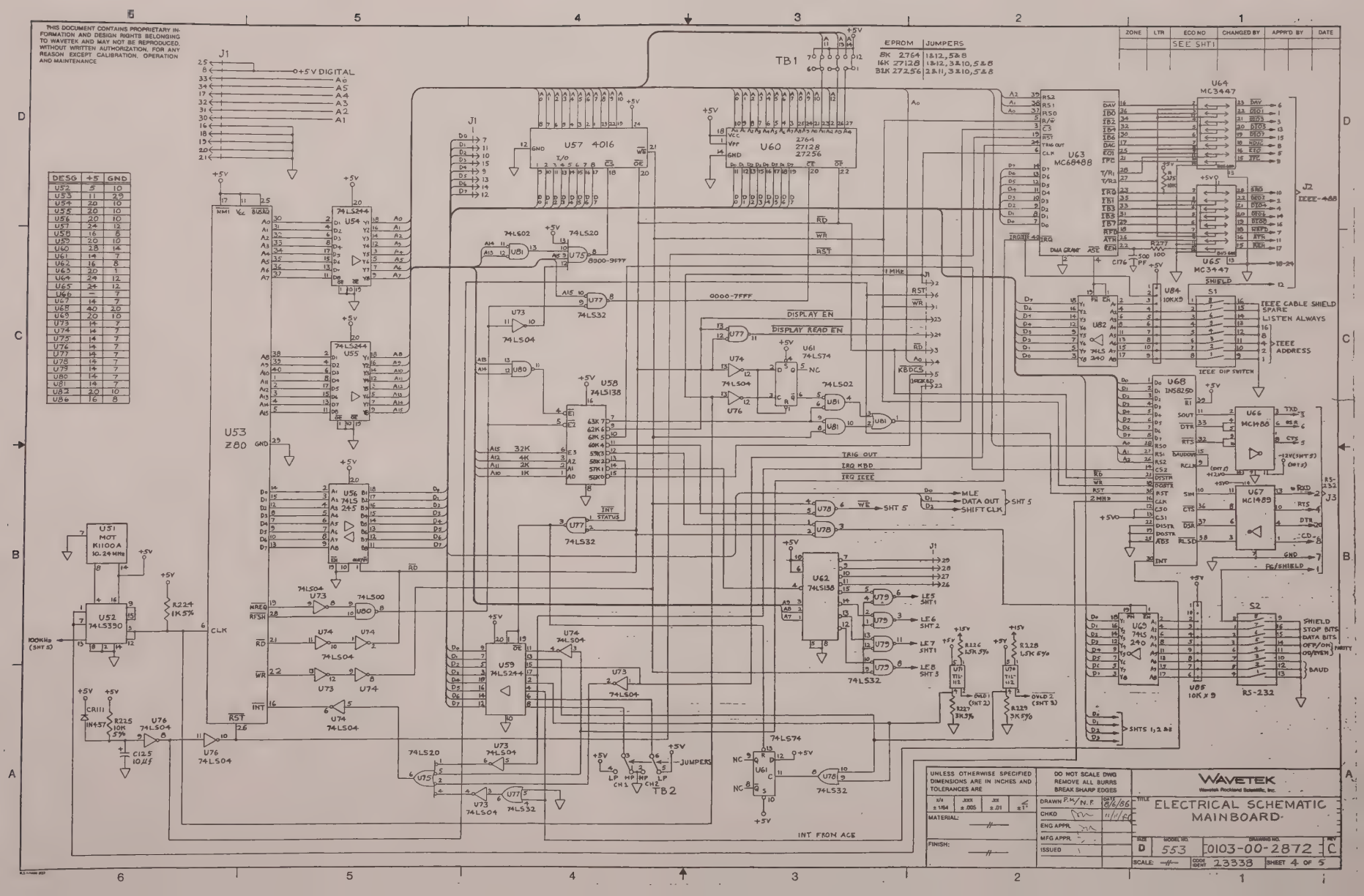

ZONE
LTR
ECO NO
CHANGED BY
APPR'D BY
DATE
SEE SHT 1
LF351
LF347
LF347
+V4
-V4
+V5
-V5
+V6
-V6
+V0
C50 .01
C51 .01
C52
C53 .01
C55
C56 .01
C57 .01
R51 20.5K
R52 5.23K
R53 20.5K
R54 20.5K
R55 60.4K
R56 5K
R57 10K 5%
R74 46.75K .5%
R75 7.027K .1%
R76 15.5K .1%
R77 20.5K
R78 9.09K
R79 20.5K
R80 20.5K
R81 20.5K
R82 1K
R83 10K 5%
R100 19.38 .1%
R101 600 .1%
R102 600Ω .1%
CR52
CR53
CR54
CR55
TP4
E6
E7
U11 9 x 47K
U15 9 x 47K
U16 9 x 47K
U17 9 x 47K
U18 9 x 47K
2N5638
CR10
CR17
CR18
CR25
CR26
CR33
CR34
CR41
CR42
CR49
C25 68 PF
C30 820 PF
C31
C27 .1
C28 .01
C32 .1
C33 .01
C34 910 PF
C35 56 PF
C36 .1
C37 .01
C38 56 PF
C39 910 PF
C40
C41 .1
C42 .01
C43 910 PF
C44 56PF
C45 .1
C46 .01
C47 56 PF
C48 910 PF
C49
K5
K6
K7
K8
K9
K10
K11
K12
K13
K14
E1
E2
E3
E4
E5
JUMPERS
AMP1 (SHT 1)
R33 21.5K
R34 4.7K 5%
R35 10Ω 5%
R36 10K 5%
R37 21.5K
R38 100K 5%
R39 1K
R40 1K
R41 1M 5%
R42 10Ω 5%
C20 22PF
C21 .1
C22 .1
C23 .1
C24 .1
C25 10μF
C26 200PF
LM339
Q5D 2N4249
OVLD 1 (SHT 4)
U21 LM324
U22 LM324
U23 74LS273
U24 74LS175
U20 75494
U28 7 x 1K
C61 .01
C62 .01
C60 .01
C164
R111 10K 5%
CR50
CR51
LE2 (SHT 5)
LE6
SHT 5
SHT 4
A
B
C
D
E
F
G
H
D0
D1
D2
D3
OUT CHAN 1 J6
R108 100K
R107 470K 5%
R109 L62K
R103 300Ω
R106 550Ω
R110 51Ω 5%
R104 4.32K
R105 2K
C59 .01
C58 .01
U19
WAVETEK
ELECTRICAL SCHEMATIC
MAINBOARD
D 553
0103-00-2872
C
23338
2 5

THIS DOCUMENT CONTAINS PROPRIETARY INFORMATION AND DESIGN RIGHTS BELONGING TO WAVETEK AND MAY NOT BE REPRODUCED WITHOUT WRITTEN AUTHORIZATION, FOR ANY REASON EXCEPT CALIBRATION, OPERATION AND MAINTENANCE

ZONE	LTR	ECO NO	CHANGED BY	APPR'D. BY	DATE
		SEE SHT 1			

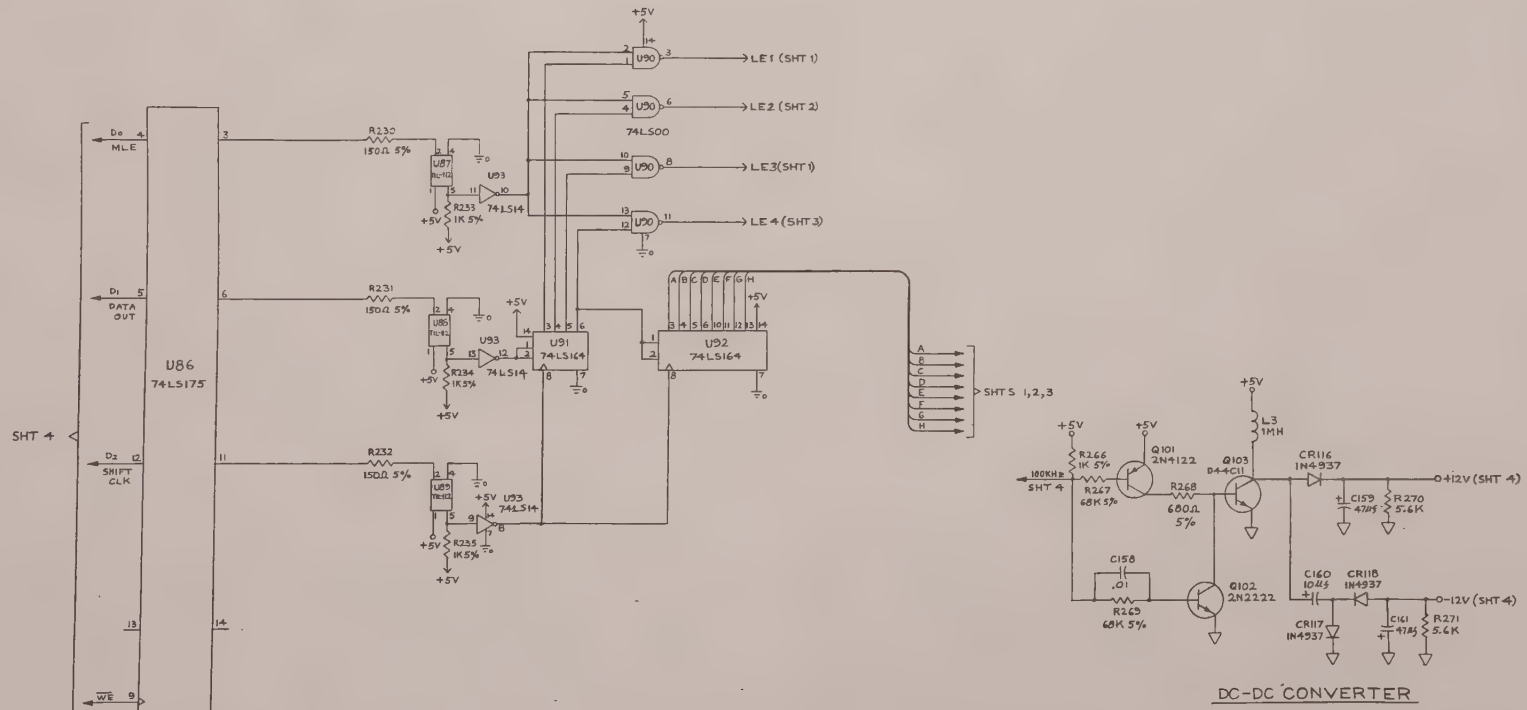


UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND TOLERANCES ARE	DO NOT SCALE DWG REMOVE ALL BURRS BREAK SHARP EDGES	WAVETEK Wavetek Rockland Scientific, Inc
x/± 1/64 | xxx ± .005 | xx ± .01 | ∠ ± 1°	DRAWN P.M./N.P. DATE 8/6/86	TITLE ELECTRICAL SCHEMATIC MAINBOARD
MATERIAL: //	CHKD [illegible] 11/11 SC	SIZE D | MODEL NO 553 | DRAWING NO 0103-00-2872 | REV C
FINISH: //	ENG APPR. [illegible]	SCALE // | CODE IDENT 23338 | SHEET 3 OF 5
	MFG APPR	
	ISSUED	


THIS DOCUMENT CONTAINS PROPRIETARY INFORMATION AND DESIGN RIGHTS BELONGING TO WAVETEK AND MAY NOT BE REPRODUCED, WITHOUT WRITTEN AUTHORIZATION, FOR ANY REASON EXCEPT CALIBRATION, OPERATION AND MAINTENANCE
ZONE | LTR | ECO NO | CHANGED BY | APPR'D BY | DATE
SEE SHT1
EPROM JUMPERS
8K 2764 1&12, 5&8
16K 27128 1&12, 3&10, 5&8
32K 27256 2&11, 3&10, 5&8
DESG +5 GND
U52 5 10
U53 11 29
U54 20 10
U55 20 10
U56 20 10
U57 24 12
U58 16 8
U59 20 10
U60 28 14
U61 14 7
U62 16 8
U63 20 1
U64 24 12
U65 24 12
U66 - 7
U67 14 7
U68 40 20
U69 20 10
U73 14 7
U74 14 7
U75 14 7
U76 14 7
U77 14 7
U78 14 7
U79 14 7
U80 14 7
U81 14 7
U82 20 10
U86 16 8
J1
0+5V DIGITAL
A0
A5
A4
A3
A2
A1
TB1
U57 4016
U60 2764 27128 27256
U63 MC68488
U64 MC3447
U65 MC3447
J2 IEEE-488
U53 Z80
U54 74LS244
U55 74LS244
U56 74LS 245
U58 74LS138
U59 74LS244
U61 74LS74
U62 74LS138
U63 74LS 240
U66 MC1488
U67 MC1489
U68 INS8250
U69 74LS 240
U82 74LS 240
U85 10K x 9
U86 16 8
U51 MOT K1100A 10.24 MHz
U52 74LS390
U73 74LS04
U74 74LS04
U75 74LS20
U76 74LS04
U77 74LS32
U78 74LS32
U79 74LS32
U80 74LS00
U81 74LS02
U86 74LS74
R224 1K 5%
R225 10K 5%
R226 1.5K 5%
R227 3K 5%
R228 1.5K 5%
R229 3K 5%
R277 500
C125 10µF
C176 .1µF
CR111 IN457
S1
S2
RS-232
IEEE CABLE SHIELD
SPARE
LISTEN ALWAYS
IEEE ADDRESS
IEEE DIP SWITCH
SHIELD
SHIELD
STOP BITS
DATA BITS
OFF/ON PARITY
ODD/EVEN
BAUD
RS-232
0000-7FFF
8000-9FFF
DISPLAY EN
DISPLAY READ EN
TRIG OUT
IRQ KBD
IRQ IEEE
INT FROM ACE
JUMPERS
LP MP HP
CH1 CH2
TB2
MLE
DATA OUT
SHIFT CLK
SHT 5
SHT1
SHT2
SHT3
SHT5
SHT6
SHT7
SHT8
SHTS 1,2 &8
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND TOLERANCES ARE
DO NOT SCALE DWG
REMOVE ALL BURRS
BREAK SHARP EDGES
MATERIAL:
FINISH:
DRAWN P.H./N.F. 8/6/86
CHKD 11/11/86
ENG APPR
MFG APPR
ISSUED
WAVETEK
Wavetek Rockland Subsidiary, Inc.
TITLE ELECTRICAL SCHEMATIC MAINBOARD
SIZE D
MODEL NO. 553
DRAWING NO. 0103-00-2872
REV C
SCALE:
CODE IDENT 23338
SHEET 4 OF 5

THIS DOCUMENT CONTAINS PROPRIETARY INFORMATION AND DESIGN RIGHTS BELONGING TO WAVETEK AND MAY NOT BE REPRODUCED, WITHOUT WRITTEN AUTHORIZATION, FOR ANY REASON EXCEPT CALIBRATION, OPERATION, AND MAINTENANCE

ZONE	LTR	ECO NO	CHANGED BY	APPR'D. BY	DATE
		SH1 SHT1			

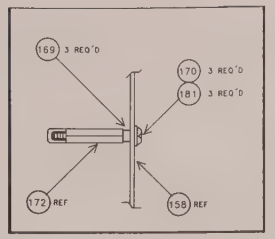


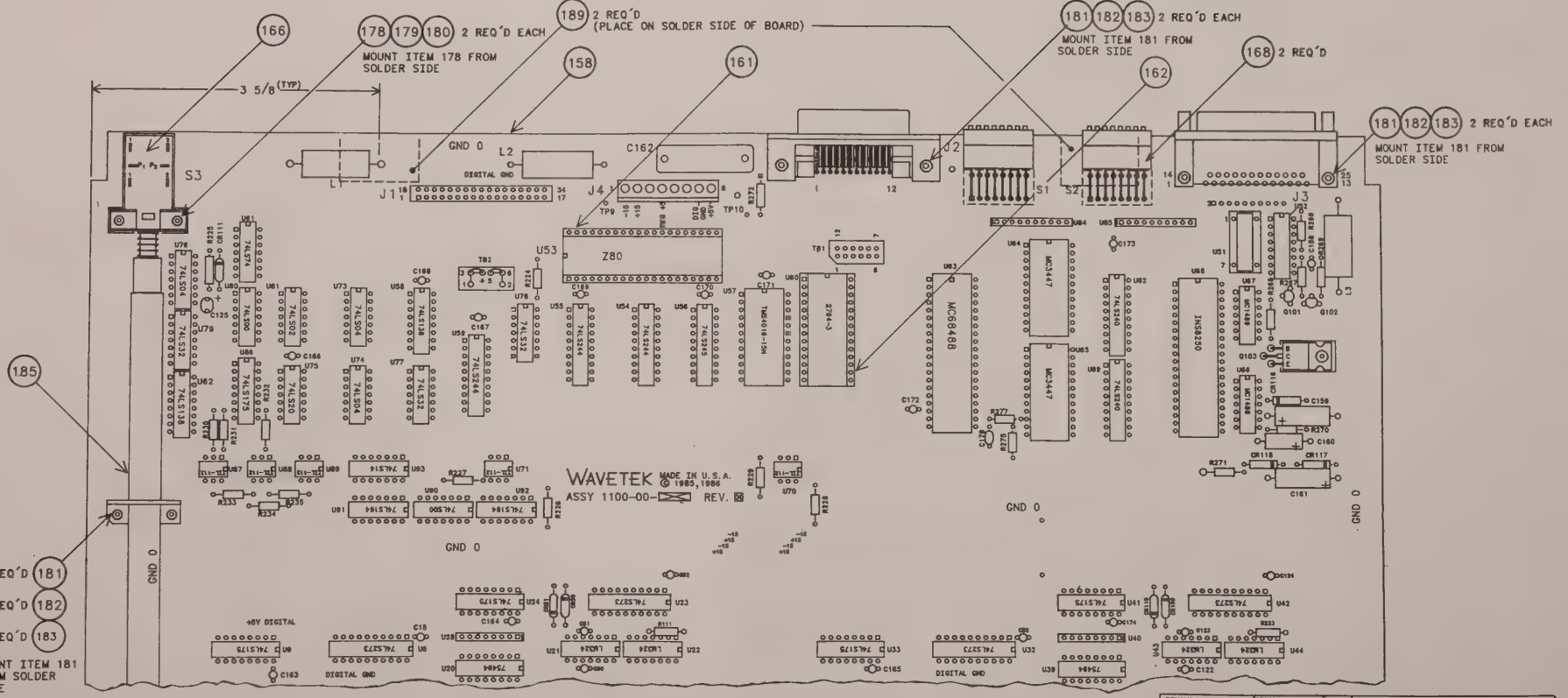
DC-DC CONVERTER

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND TOLERANCES ARE	DO NOT SCALE DWG REMOVE ALL BURRS BREAK SHARP EDGES	WAVETEK Wavetek Rockland Scientific, Inc
x/± 1/64 .xxx ± .005 xx ± .01 ∠ ±1°	DRAWN P.M./N.P. DATE 8/5/86	TITLE ELECTRICAL SCHEMATIC MAINBOARD
MATERIAL: —	CHKD	
FINISH: —	ENG APPR	SIZE D MODEL NO. 553 DRAWING NO. 0103-00-2872 REV C
	MFG APPR	SCALE: — CODE IDENT 23338 SHEET 5 OF 5
	ISSUED	

THIS DOCUMENT CONTAINS PROPRIETARY INFORMATION AND DESIGN RIGHTS BELONGING TO WAVETEK AND MAY NOT BE REPRODUCED, WITHOUT WRITTEN AUTHORIZATION, FOR ANY REASON EXCEPT CALIBRATION, OPERATION, AND MAINTENANCE.

ZONE	LTR	ECO NO	CHANGED BY	APPRD BY		DATE
	A	PROTO		R.H		8/2/85
	B	RELEASE		R.H.		11/22/85
	C	ECO 2089	N.P. 12/4/85	D.S.	S.R.	
	D	ECO 2083	N.P. 2/7/86	P.M.		
	E	ECO 2121	N.P. 4/14/86	P.M.		
	F	ECO 2124	N.P. 4/29/86	P.M.		
	G	ECO 2146	N.P. 6/6/86	P.M.		6/12/86
	H	ECO 2197	N.P. 7/21/86	P.M.		
	J	ECO2231	N.P. 8/26/86	DM	3M	9/19/86
	K	ECO 7802	SD 11-19-86	DM		11-21-86



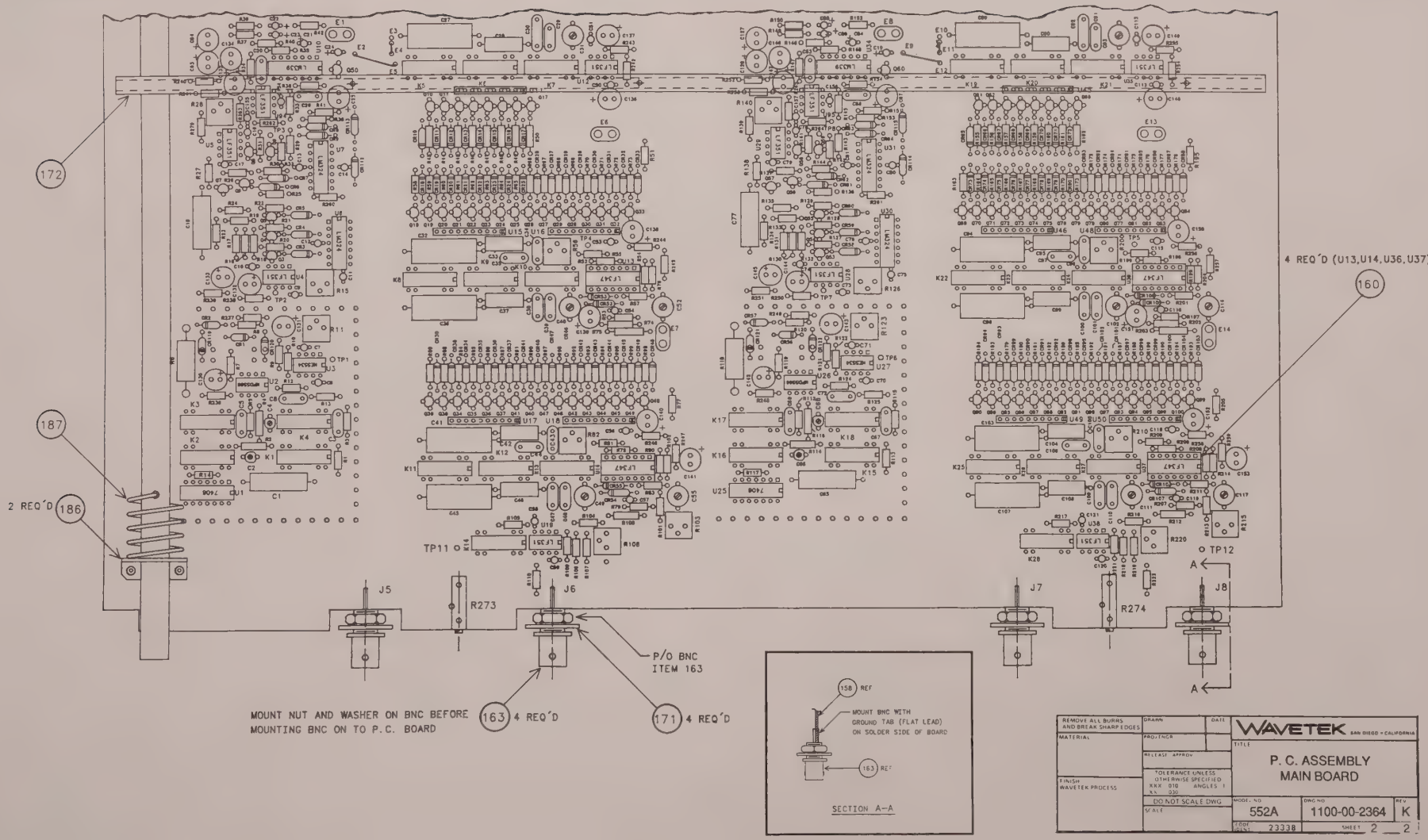


FOR OTHER HALF OF BOARD SEE SHEET 2

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN	DATE	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL	PROJENGR		TITLE: P. C. ASSEMBLY MAIN BOARD
FINISH WAVETEK PROCESS	RELEASE APPROV		
	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX .010 ANGLES ±1 XX .030		
	DO NOT SCALE DWG		MODEL NO 552A; DWG NO 1100-00-2364; REV K
	SCALE		CODE IDENT 23338; SHEET 1 OF 2

THIS DOCUMENT CONTAINS PROPRIETARY INFORMATION AND DESIGN RIGHTS BELONGING TO WAVETEK AND MAY NOT BE REPRODUCED, WITHOUT WRITTEN AUTHORIZATION, FOR ANY REASON EXCEPT CALIBRATION, OPERATION, AND MAINTENANCE.

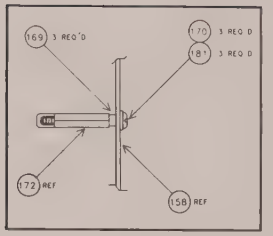
FOR OTHER HALF OF BOARD SEE SHEET 1

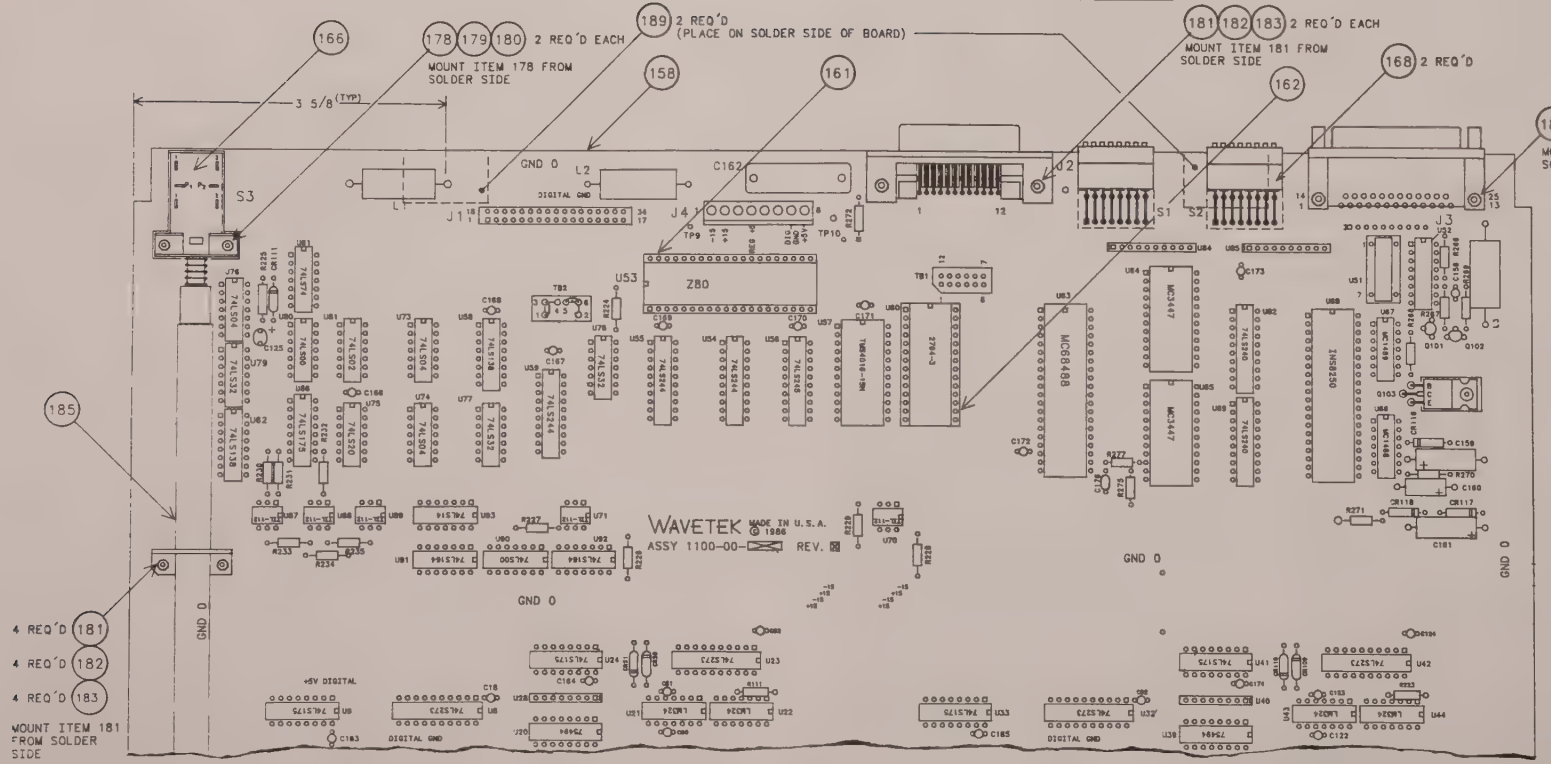


REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN	DATE	WAVETEK SAN DIEGO - CALIFORNIA
MATERIAL	PROJ ENGR		TITLE: P. C. ASSEMBLY MAIN BOARD
	RELEASE APPROV		
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX .010 ANGLES ± XX .030		MODEL NO: 552A
	DO NOT SCALE DWG		DWG NO: 1100-00-2364 REV: K
	SCALE		FSCM NO: 23338 SHEET 2 OF 2

THIS DOCUMENT CONTAINS PROPRIETARY INFORMATION AND DESIGN RIGHTS BELONGING TO WAVETEK AND MAY NOT BE REPRODUCED, WITHOUT WRITTEN AUTHORIZATION, FOR ANY REASON EXCEPT CALIBRATION, OPERATION, AND MAINTENANCE.

ZONE	LTR	ECO NO	CHANGED BY	APPRD BY	DATE
	A	RELEASE			
	B	7802	SD 11-14-86		11-21-86
	C	7853	SD 2-9-87		
	D	7971	SD 2-9 87		



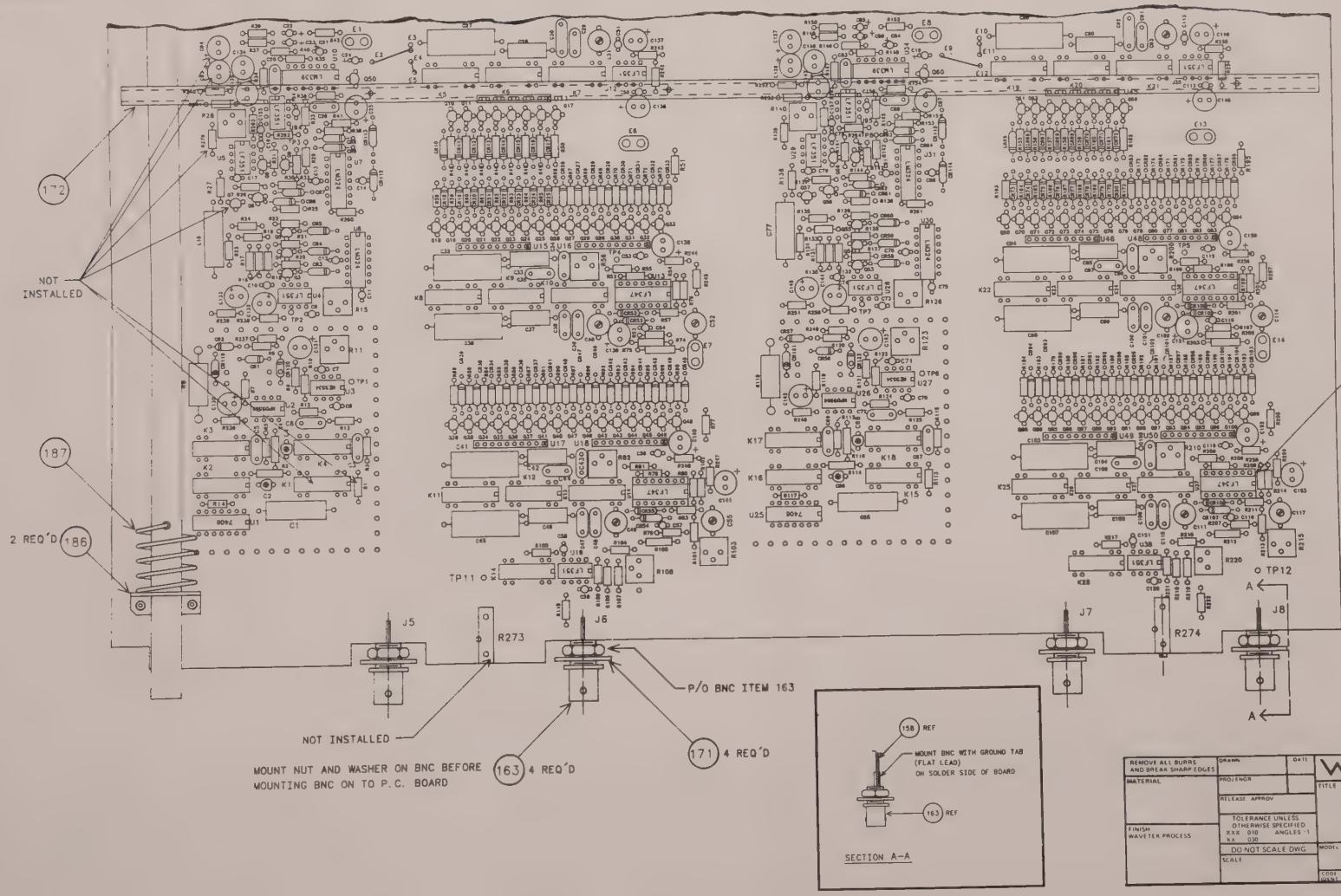


FOR OTHER HALF OF BOARD SEE SHEET 2

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN	DATE	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL	PROJ ENGR		TITLE: P. C. ASSEMBLY MAIN BOARD
	RELEASE APPROV		
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX .010 ANGLES ± XX .030		
	DO NOT SCALE DWG		MODEL NO 553A / DWG NO 1100-00-2872 / REV D
	SCALE		CODE IDENT 23338 / SHEET 1 OF 2

THIS DOCUMENT CONTAINS PROPRIETARY INFORMATION AND DESIGN RIGHTS BELONGING TO WAVETEK AND MAY NOT BE REPRODUCED, WITHOUT WRITTEN AUTHORIZATION, FOR ANY REASON EXCEPT CALIBRATION, OPERATION, AND MAINTENANCE.

FOR OTHER HALF OF BOARD SEE SHEET 1



REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN	DATE	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL	PROJENGR		TITLE: P. C. ASSEMBLY MAIN BOARD
	RELEASE APPROV		
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX .010 ANGLES ±1 XX .030		
	DO NOT SCALE DWG		MODEL NO 553A; DWG NO 1100-00-2872; REV D
	SCALE		CODE IDENT 23338; SHEET 2 OF 2

THIS DOCUMENT CONTAINS PROPRIETARY INFORMATION AND DESIGN RIGHTS BELONGING TO WAVETEK AND MAY NOT BE REPRODUCED FOR ANY REASON EXCEPT CALIBRATION, OPERATION AND MAINTENANCE WITHOUT WRITTEN AUTHORIZATION

REV	ECN	BY	DATE	APP

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO	QTY/PT
[illegible]	C: FX MONO 01UF +80 -20% 30V	SR215E103ZAT	AVX	100 3105	1
C10 C11 C112 C113 C115 C116 C118 C119 C12 C120 C121 C122 C123 C124 C13 C14 C134 C135 C136 C137 C16 C163 C164 C165 C166 C167 C168 C169 C17 C170 C171 C172 C173 C174 C18 C50 C51 C53 C54 C56 C57 C58 C59 C6 C60 C61 C62 C7 C70 C71 C73 C74 C75 C76 C78 C79 C80 C81 C82 [illegible]	C: FX MONO 0 1UF 50V 10%	SR215E104ZAT	AVX	100 4102	60
C8 C72	CAP,FX VALUE,DP MICA 12PF 5% -20+100PPM/C 500V	CM05ED120J03	CDE	101 0120	2
C20 C83	CAP,FX VALUE,DP MICA 22PF 5% -20+100PPM/C 500V	[illegible]	CDE	101 0220	2
C100 C106 C109 C35 C38 C44 C47 C97	CAP FX VAL,DP MICA 36PF 5% -20+100PPM/C 500V	CM05ED360J03	CDE	101 0360	8
C29 C91	CAP FX VAL,DP MICA 68PF 5% -20+100PPM/C 500V	[illegible]	CDE	101 0680	2
C9 C69	CAP FX VAL,DP MICA 100PF 5% 0 TO +70PPM/C 300V	CM05FD101J03	CDE	101 1100	2
[illegible]	CAP FX VAL,DP MICA 200PF 5% 0 TO	CM05FD201J03	CDE	101 1200	2

WAVETEK PARTS LIST	TITLE: ASSY, MAIN BOARD	[illegible] 1100-00-2364	REV
	PAGE 1		

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO	QTY/PT
C86	35V				
C125 C126 C127 C128 C129 C130 C131 C132 C133 C134 C135 C136 C137 C138 C139 C140 C141 C142 C143 C144 C145 C146 C147 C148 C149 C150 C151 C152 C153 C29 C62 [illegible]	C FX TANT 10UF 20% 20V	T368B106M025A6	KEMET	109 6100	33
C160	C: FX ELECT 10UF 25V	[illegible]	MEPCO	109 6102	1
C199 C161	C: FX ELECT 47UF 20% 63V	[illegible]	BIECO	109 6470	2
R133 R144 R19 R30	R: FX MFLM 200 OHM 1% 1/10W T2	RN55C2000F	UNCEM	110 2001	4
R106 R131 R17 R218	R: FX MFLM 750 OHM 1% 1/10W T2	[illegible]	UNCEM	110.7501	4
R125 R13 R146 R150 R39 R40	R: FX MFLM 1 00K 1% 1/10W T2	RN55C1001F	UNCEM	111 1001	6
R100 R102 R212 R214	R: FX MFLM 1.344K 1% 1/8W T2			111 1349	4
R109 R130 R16 R221	R: FX MFLM 1 62K 1% 1/8W T0	RN55C1621F	UNCEM	111 1620	4
R132 R143 R18 R29	R: FX MFLM 1 82K 1% 1/8W T0	RN55C1821F	UNCEM	111 1820	4

WAVETEK PARTS LIST	TITLE: ASSY, MAIN BOARD	ASSEMBLY NO 1100-00-2364	REV
	PAGE 3		

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO	QTY/PT
R115 R3	R: FX MFLM 10 0K 1% 1/10W T2	[illegible]	UNCEM	112 1001	2
[illegible]	R: FX MFLM 15 30K 1% 1/8W T0	HA55 100PPM	HYMEG	112 1399	2
R12 R124	R: FX MFLM 16 9K 1% 1/8W T0	RN55C1692F	UNCEM	112 1690	2
R157 R45	R: FX MFLM 17 8K 1% 1/8W T0	RN55C1782F	UNCEM	112 1780	2
R195 R197 R198 R205 R207 R208 R209 R51 R53 R54 R77 [illegible]	R: FX MFLM 20 5K 1% 1/8W T0	[illegible]	UNCEM	[illegible]	14
R138 R46	R: FX MFLM 35 7K 1% 1/8W T0	RN55C3572F	UNCEM	112 3570	2
R199 R47	R: FX MFLM 44 2K 1% 1/8W T0	RN55C4422F	UNCEM	112 4420	2
[illegible]	R: FX MFLM 46 75K 1% 1/8W T0	CR125 100PPM	CTLRE	112 4678	2
R101 R213	R: FX MFLM 90 00K 1% T10			112 9006	2
R199 R35	R: FX MFLM 60 4K 1% 1/10W T2	RN55C6042F	UNCEM	112 6041	2
R160 R48	R: FX MFLM 88 7K 1% 1/8W T0	RN55C8872F	UNCEM	112 8870	2

WAVETEK PARTS LIST	TITLE: ASSY, MAIN BOARD	ASSEMBLY NO 1100-00-2364	REV
	PAGE 5		

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO	QTY/PT
	+70PPM/C 300V				
C3 C67	CAP,FX VAL,DP MICA 390PF 5% 0 TO+70PPM/C 300V	CM03FD391J03	CDE	101 1390	2
C30 C92	CAP,FX VAL,DIP MICA 820PF 1% 0 TO+70PPM/C 300V	CD15FC821F03	CDE	101 1821	2
C101 C105 C110 C34 C39 C43 [illegible]	CAP,FX VAL,DIP MICA 910PF 1% 0 TO+70PPM/C 100V	CD15FA911F03	CDE	101 1910	8
C104 C108 C28 C30 C37 C42 C46 C90 C95 C99	C: FX PLYSTY 01UF - 3+0%	PS3PC0103E	AMRAD	104 3106	10
[illegible]	C: FX PLYCRB 0 1UF - 3+0% 100V	MPABPC0104E	AMRAD	104 4103	2
C103 C107 C32 C36 C41 C45 [illegible]	C: FX PLYSTY 0 1UF 50V SET	PSM0104F-M8	AMRAD	104 4107	4
C1 C15 C49 C77	C: FX PLSTR 47UF 5% 180H	XA2C474J	ISMEL	105 4470	4
C2 C4 C66 C68	C VAR CER 3 5-18PF 250V	9373	JACO	108 0180	4
C102 C111 C114 C117 C31 C40 C48 C52 C55 C93	C VAR CER 15-60PF	538-011-F	MILGY	108 0600	10
C19 C21 C22 C23 C24 C84 C85	C. FX TANT 10UF 20%	T368A104M035A6	KEMET	109 4100	8

WAVETEK PARTS LIST	TITLE: ASSY, MAIN BOARD	ASSEMBLY NO 1100-00-2364	REV
	PAGE 2		

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO	QTY/PT
R105 R217	R: FX MFLM 2.00K 1% 1/10W T2	[illegible]	UNCEM	111 2001	2
R118 R6	R: FX MFLM 2.40K 5% 2W 200PPM	FP42 2.4K 5% 2W 200PPM	CORNO	111 2403	2
R10 R121 R122 R9	R: FX MFLM 2.87K 1% 1/10W T2			111 2871	4
R263 R265	R: FX MFLM 3.24K 1% 1/8W T0			111 3240	2
R134 R23 R262 R264	R: FX MFLM 3.92K 1% 1/10W T2	NA	NA	111 3921	4
R104 R216	R: FX MFLM 4.32K 1% 1/10W T2	RN55C4321F	UNCEM	111.4321	2
R139 R43	R: FX MFLM 4.42K 1% 1/10W T2	RN55C4421F	UNCEM	111 4421	2
R135 R24	R: FX MFLM 4.99K 1% 1/10W T2	RN55C4991F	UNCEM	111 4991	2
[illegible]	R: FX MFLM 7.027K 1% 1/8W T0	HA55 100PPM	HYMEG	111 7028	2
[illegible]	R: FX MFLM 8.87K 1% 1/8W T0	RN55C8871F	NA	111 8870	2
R145 R149 R206 R33 R37 R78	R: FX MFLM 9.09K 1% 1/8W T0			111 9090	6

WAVETEK PARTS LIST	TITLE: ASSY, MAIN BOARD	ASSEMBLY NO 1100-00-2364	REV
	PAGE 4		

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO	QTY/PT
R117 R5	R: FX MFLM 100K 1% 1/10W T2	RN55C1003F	UNCEM	113 1001	2
R161 R49	R: FX MFLM 178K 1% 1/8W T0	RN55C1783F	UNCEM	113 1780	2
R162 R50	R: FX MFLM 357K 1% 1/8W T0	RN55C3573F	CTLRE	113 3570	2
R114 R116 R2 R4	R: FX MFLM 900K 1% 1/10W T2			113 9009	4
R140 R132 R35 R42	R: FX CFLM 10 OHM 5% 1/4W			116 0101	4
R110 R221	R: FX CFLM 51 OHM 5% 1/4W			116.0911	2
R1 R113	R: FX CFLM 82 OHM 5% 1/4W			116 0821	2
R234 R237 R238 R239 R240 R241 R242 R243 R244 R245 R246 R247 R248 R249 R250 R251 R252 R253 R254 R255 R256 R257 R258 R259	R: FX CFLM 100 OHM 5% 1/4W			116 1101	24
R230 R231 R232	R: FX CFLM 130 OHM 5% 1/4W			116 1131	3
R268	R: FX CFLM 680 OHM 5% 1/4W			116.1681	1

WAVETEK PARTS LIST	TITLE: ASSY, MAIN BOARD	ASSEMBLY NO 1100-00-2364	REV
	PAGE 6		

NOTE UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN	DATE	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL	PROJ ENGR		TITLE: PARTS LIST MAIN BOARD ASSEMBLY
	RELEASE APPROV		
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX .010 ANGLES 1 XX .030		MODEL NO 552A
	DO NOT SCALE DWG		DWG NO 1100-00-2364 REV K
	SCALE		CODE IDENT 23338 SHEET 1 OF 3

THIS DOCUMENT CONTAINS PROPRIETARY INFORMATION AND DESIGN RIGHTS BELONGING TO WAVETEK AND MAY NOT BE REPRODUCED FOR ANY REASON EXCEPT CALIBRATION, OPERATION AND MAINTENANCE WITHOUT WRITTEN AUTHORIZATION

REV	ECN	BY	DATE	APP

REFERENCE [illegible]	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO	QTY/. T
R224 R233 R234 R235 R266	R FX CFLM 1 0K OHM 5% 1/8W			116 2100	5
R226 R228	R FX CFLM 1 5K OHM 5% 1/4W			116 2151	2
R227 R229	R FX CFLM 3 0K OHM 5% 1/4W			116 2301	2
R119 R120 R147 R24 R7 R8	R FX CFLM 4 7K OHM 5% 1/4W			116 2471	6
R270 R271	R FX CFLM 5 6K OHM 5% 1/4W			116 2561	2
R111 R153 R201 R211 R223 R225 R273 R36 R37 R83	R FX CFLM 10K OHM 5% 1/4W			116 3101	10
R127 R128 R129 R136 R137 R141 R142 R20 R21 R22 [illegible] R26 R31 R32	R FX CFLM 47K OHM 5% 1/4W			116 3471	14
R266 R269	R FX CFLM 68K OHM 5% 1/4W			116 3681	2
R112 R139 R154 R272 R38	R FX CFLM 100K OHM 5% 1/4W			116 4101	5
R107 R117 R138 R14 R151 R219 R27 R41	R FX CFLM 1 0M OHM 5% 1/4W			116 5101	8
R103 R11 R123 R215	R VAR CMT 500 OHM	72PR500	BECK	118 1503	4

WAVETEK PARTS LIST | TITLE: ASSY. MAIN BOARD | ASSEMBLY NO 1100-00-2364 | REV | PAGE 7

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO	QTY/PT
	(75494)				
U70 U71 U87 U88 U89	U OPTO-ISOLATOR (TIL-112)	TIL-112	TI	120 9112	5
SW3	SWITCH ASSY-552	552-2398	WVTK	1202-00-2398	1
U1 U23	U HEX INVERT DRIVER O/C			122 7406	2
U38 U62	U 3 TO 8 LINE DECOD (74LS138)	74LS138N/AT	NSC	125 0115	2
U23 U32 U42 U8	U OCT D-FLIP W/CLR (74LS273)			125 0139	4
U69 [illegible]	U OCT BUF INV 3-ST (74LS240)	74LS240N/PJ	TI	125 0144	2
U54 U55 U59	U OCT BUF 3-ST (74LS244)	74LS244N/S2B	SIG	125 0153	3
U56	U OCT BUS XCVR 3ST (74LS245)	74LS245N/PJ	TI	125 0154	1
U80 U90	U QUAD 2 IN NAND GATE	74LS00N/S2B	TI	125 7400	2
U81	U QUAD 2IN NOR GATE	74LS02N/S	TI	125 7402	1
U73 U74 U76 U93	U HEX INVERTER	74LS04N/S2B	SIG	125 7404	4
U75	U DUAL 4 IN NAND	74LS20NDS	RAYTH	125 7420	1

WAVETEK PARTS LIST | TITLE: ASSY. MAIN BOARD | ASSEMBLY NO 1100-00-2364 | REV | PAGE 9

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO	QTY/PT
CR14 CR15 CR16 CR17 CR18 CR19 CR20 CR21 CR22 CR23 [illegible] CR25 CR26 CR27 CR28 CR29 CR3 CR30 CR31 CR32 CR33 CR34 CR35 CR36 CR37 CR38 CR39 CR4 CR40 CR41 CR42 CR43 CR44 CR45 CR46 CR47 CR48 CR49 CR5 CR50 CR51 CR52 CR54 CR58 CR59 CR6 CR60 CR61 CR62 CR63 CR64 CR65 CR66 CR67 CR68 CR69 CR7 CR70 CR71 CR72 CR73 CR74 CR75 CR76 CR77 CR78 CR79 CR8 CR80 CR81 CR82 CR83 CR84 CR85 CR86 CR87 CR88 CR89 CR9 CR90 CR91 CR92 CR93 CR94 CR95 CR96 CR97 CR98 CR99					
Q102	Q SIL NPN (2N2222)	2N2222A	MOT	134 2222	1
Q101	[illegible] SIL PNP (2N4122)			136 4122	1
[illegible]	Q SIL PNP (2N4249)			136 4249	2
U2 U26	Q: DL MATCH FET (NPD-5566)	NPD-5566	NSC	138 5566	2
Q10 Q100 Q11 Q12 Q13 Q14 Q15 Q16 Q17 Q18 Q19 Q20 Q21 Q22 Q23 Q24 Q25 Q26 Q27 Q28 Q29 Q3 Q30 Q31 Q32 Q33 Q34 Q35 Q36 Q37 Q38 Q39 Q4 Q40	Q FET N-CHAN JCT	2N5638-5	NSC	138 5638	94

WAVETEK PARTS LIST | TITLE: ASSY. [illegible] | ASSEMBLY NO 1100-00-2364 | REV | PAGE 11

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO	QTY/PT
[illegible]	3/8SQ FM				
[illegible]	R VAR CMT 1 0K 3/8SQ FM	72PR1K	BECK	118 2102	2
R200 R56	R VAR CMT 5 0K 3/8SQ FM	72PR5K	BECK	118 2502	2
R126 R140 R15 R28	R VAR CMT 10K 3/8SQ FM	72PR10K	BECK	118 3101	4
[illegible]	R VAR CMT 100K 3/8SQ FM			118 4103	2
U12 U19 U28 U29 U35 U36 U4 U5	U LIN BIFET OP-AMP DIL LF351	LF351N	NSC	120 1017	8
U27 U3	U LIN OP-AMP DIL (NE5534A)	SA5534AN	SIG	120 1018	2
U13 U14 U34 U37	SPK U QD LIN BIFET OP-AMP (SEL347			120 2007	4
U21 U22 U30 U31 U43 U44 U6 U7	U QD LIN OP-AMP (LM324N)	LM324N	NSC	120 2324	8
U64 U65	U IEEE BUS XCVR (MC3447P)	MC3447P	MOT	120 2447	2
U10 U34	U QUAD ANAL VOLT COMP (LM339)	LM339N	MOT	120 3339	2
U20 U39	U HEX MOS-LED DRIVER	75494N	NSC	120 4494	2

WAVETEK PARTS LIST | TITLE: ASSY. MAIN BOARD | ASSEMBLY NO 1100-00-2364 | REV | PAGE 8

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO	QTY/PT
	GATE				
U77 U78 U79	U QUAD 2 IN OR GATE	74LS32N/S2B	SIG	125 7432	3
U61	U DUAL TYPE D FLIP FLOP	74LS74N/PJ	SIG	125 7474	1
U28 U40	U: PULL UP NET 1K 2% X7 SIP	4308R-101-102	BOURN	128 2105	2
U83 U84 U85	U PULL UP NET 10K 2% X9 SIP	110A103	AB	128 3104	3
U60				129 3030	1
U57	U SRAM 2048 X 8 NMOS	TMS4016-15N	TI	129 3032	1
U53	MICRO PROCESSOR (2 MHZ. Z80)	MK3880N	MOSTK	129 3201	1
U63	MC68488-M4	MC68488P	MOT	129 3202	1
CR116 CR117 CR118	CR SIL RC7 600PIV 1A (1N4937)			130 4110	3
CR1 CR106 CR108 CR2 CR53 CR55 CR56 CR57	CR SL ZR 5 1V 5% 400MW 1N751A			131 9510	8
CR10 CR100 CR101 CR102 CR103 CR104 CR105 CR107 CR109 CR11 CR111 CR112 CR113 CR114 CR115 CR119 CR12 CR120 CR121 CR122 CR13	CR SL LW LK 70PIV 200MW 1N457			132 0457	110

WAVETEK PARTS LIST | TITLE: ASSY. MAIN BOARD | ASSEMBLY NO 1100-00-2364 | REV | PAGE 10

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO	QTY/PT
K1 K10 K11 K12 K13 K14 K15 K16 K17 K18 K2 K22 K23 K24 K25 K26 K27 K3 K4 K8 K9	RELAY REED DIP 2A W/DIODE 5V	1303-7-1	WABSH	173 1307	18
J2	CONNECTOR, 9P1B, RT ANGLE PC MOUNT	68519-001	BERG	2100-02-0198	1
J3	CONNECTOR, D-SUB, HDR, P C MOUNT	67711-025	BERG	2100-02-0199	1

WAVETEK PARTS LIST | TITLE: ASSY. MAIN BOARD | ASSEMBLY NO. 1100-00-2364 | REV | PAGE 12

NOTE UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN	DATE	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL	PROJ/ENGR		TITLE: PARTS LIST MAIN BOARD ASSEMBLY
	RELEASE APPROV		
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ± .010 ANGLES ± XX ± .030		
	DO NOT SCALE DWG	MODEL NO 552A	DRG NO 1100-00-2364 REV
	SCALE	CODE IDENT 23338	SHEET 2 OF 3

BISHOP GRAPHICS/ACCUPRESS RECORDER NO. A 3894

THIS DOCUMENT CONTAINS PROPRIETARY INFORMATION AND DESIGN RIGHTS BELONGING TO WAVETEK AND MAY NOT BE REPRODUCED FOR ANY REASON EXCEPT CALIBRATION, OPERATION, AND MAINTENANCE WITHOUT WRITTEN AUTHORIZATION

REV	ECN	BY	DATE	APP

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO	QTY/PT
SW1 SW2	8 DIP 8 POLE 2 POS	[illegible]	GRAHL	342 8100	2
J3 J6 J7 J8	CONN COAX BLKHD RECPT 180L	31-010	AMPH	351 0006	4
E1 E13 E14 E6 E7 E8	PLUG SHORTING (LOW PROF)	4612872-01-03-10	CTC	352 0202	6
XE1 XE13 XE14 XE6 XE7 XE8	SOCKET JMPR (USE W/352 0202)	4303327-01-0300	CTC	353 0104	12
XU13 XU14 XU36 XU37	SOCKET IC 14PIN DIP ST			353 1403	4
XS1 XS2	SOCKET IC 16PIN DIP HDR	16-823-90	ARIES	353 1603	2
XU60	SOCKET IC 28PIN DIP ST			353 2800	1
XU53	SOCKET IC 40PIN DIP ST			353 4001	1
J1	CONN TERM 34 PIN DIL ST	929665-01-17	A/P	354 0005	1
TP1 TP2 TP3 TP4 TP5 TP6 TP7 TP8	CONN TERM PIN .025 SQ .[illegible]003	W239-025-3000	A/B	354 0007	8
J4	CONN TERM 8 POS (MOLEX)			354 0016	1

WAVETEK PARTS LIST | TITLE: ASSY. MAIN BOARD | ASSEMBLY NO 1100-00-2364 | REV | PAGE 13

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO	QTY/PT
R180 R188 R85 R94	RES.MF,1/8W, 1%,5 304 H	MN55-5 304K- 1-100	HYMEQ	4799-00-0109	4
R181 R189 [illegible] R94	RES.MF,1/8W, 1%,10 64 K	MN55-10 64K- 1-100	HYMEQ	4799-00-0110	4
R182 R190 R87 R95	RES.MF,1/8W, 1%,21 31 K	MN55-21 31K- 1-100	HYMEQ	4799-00-0111	4
R183 R191 R88 [illegible]	RES.MF,1/8W, 1%,26 64 H	MN55-26 64K- 1-100	HYMEQ	4799-00-0112	4
R184 R192 R89 [illegible]	RES.MF,1/8W, 1%,53 32 H	MN55-53 32K- 1-100	HYMEQ	4799-00-0113	4
R185 R193 R90 R98	RES.MF,1/8W, 1%,106 7 K	MN55-106 7K- 1-100	HYMEQ	4799-00-0114	4
R186 R194 R91 [illegible]	RES.MF,1/8W, 1%,213 4 H	MN55-213 4K- 1-100	HYMEQ	4799-00-0115	4
R179 R187 R84 [illegible]	RES.MF,1/8W, 1%,2 637 H	MN55-2 637K- 1-100	HYMEQ	4799-00-0116	4
R165 R173 R60 R68	RES.MF,1/8W, 1%,7 630 H	MN55 7 630K- 1-100	HYMEQ	4799-00-0117	4
R166 R174 R61 R69	RES.MF,1/8W, 1%,15 30 K	MN55-15 30K- 1-100	HYMEQ	4799-00-0118	4
R167 R175 R62 R70	RES.MF,1/8W, 1%,19 12 K	MN55-19 12K- 1-100	HYMEQ	4799-00-0119	4

WAVETEK PARTS LIST | TITLE: ASSY. MAIN BOARD | ASSEMBLY NO [illegible] | REV | PAGE 15

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO	QTY/PT
NONE	M SCR SS PHP 2-56 X 1/4 PH			385 2042	2
NONE	M SCR SS PHP 4-40 X 3/8 PH			385 4062	8
NONE	M SCR SS PHP 4-40X7/16 100FH			385 4074	2
NONE	NUT HEX SS 2-56 X 5/32AB			387 2051	2
NONE	NUT HEX SS 4-40 X 1/4AF			387 4081	8
NONE	WASHER FLAT STL CAD 94			388 0040	8
NONE	WASHER SPLT LK STNLS #8			388 1082	2
NONE	SPR THD M/F 1/4HX 4-40X5/8	8219	SMITH	389 2031	3
NONE	GUIDE PIN ASSY FEM METRIC	552633-3	AMP	389 7004	2
R169 R177 R64 R72	RES.MF,1/8W, 1%,76 60 K	MN55-76 60K- 1-100	HYMEQ	4799-00-0107	4
R170 R178 R65 R73	RES.MF 1/8W, 1%,133 2 [illegible]	MN55-133 20K- 1-100	HYMEQ	4799-00-0108	4

WAVETEK PARTS LIST | TITLE: ASSY. MAIN BOARD | ASSEMBLY NO 1100-00-2364 | REV | PAGE 14

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO	QTY/PT
R168 R176 R63 R71	RES.MF,1/8W, 1%,38 30 H	MN55-38 30K- 1-100	HYMEQ	4799-00-0120	4
R163 R171 R58 R66	RES.MF,1/8W, 1%,1 885 H	MN55-1 885K- 1-100	HYMEQ	4799-00-0121	4
R164 R172 R59 R67	RES.MF,1/8W, 1%,3 800 K	MN55-3 800K- 1-100	HYMEQ	4799-00-0122	4
[illegible]	TRANS.NPN.PLANAR [illegible]	D44C11	NEC	4902-04-4110	1
U51	IC.OSC 10 24MHZ	K1100-A	MOT	[illegible]	1
U66	IC.QUAD LINE DRIVER,RS-232C	MC1488	MOT	[illegible]	1
U67	IC.QUAD LINE RECEIVER,RS-232C	MC1489L	MOT	[illegible]	1
U91 U92	TTL.8B BIPO SHET REG	74LS164	TI	8007-41-6410	2
U24 U33 U41 U86 U9	TTL,D-F/F,QUAD	74LS175	TI	8007-41-7510	5
U52	TTL,CNTR.DUAL 4B DCD	74LS390	TI	8007-43-9010	1

WAVETEK PARTS LIST | TITLE: ASSY. MAIN BOARD | ASSEMBLY NO 1100-00-2364 | REV | PAGE 16

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN	DATE	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL	PROJENGR		TITLE: PARTS LIST MAIN BOARD ASSEMBLY
FINISH WAVETEK PROCESS	RELEASE APPROV		
	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ±.010 XX ±.030 ANGLES ±1		
	DO NOT SCALE DWG		MODEL NO 552A; DWG NO 1100-00-2364; REV K
	SCALE		CODE IDENT 23338; SHEET 3 OF 3

NOTE UNLESS OTHERWISE SPECIFIED

B-SHOP GRAPHICS/ACCUPRESS FORDER NO A-3364

THIS DOCUMENT CONTAINS PROPRIETARY INFORMATION AND DESIGN RIGHTS BELONGING TO WAVETEK AND MAY NOT BE REPRODUCED FOR ANY REASON EXCEPT CALIBRATION, OPERATION, AND MAINTENANCE WITHOUT WRITTEN AUTHORIZATION

REV	ECN	BY	DATE	APP

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO	QTY/PT
MDME	SCHEMATIC, MAINBOARD 553	0103-00-2872	WVTK	0103-00-2872	1
C158	C: FX MDND .01UF +80 -20% 50V	SR215E103ZAT	AVX	100.3105	1
C10 C11 C112 C113 C115 C116 C118 C119 C12 C120 C121 C122 C123 C124 C13 C14 C154 C155 C156 C157 C16 C163 C164 C165 C166 C167 C168 C169 C17 C170 C171 C172 C173 C174 C18 C50 C51 C53 C54 C56 C57 C58 C59 C6 C60 C61 C62 C7 C70 C71 C73 C74 C75 C76 C78 C79 C80 C81 C82 C9	C: FX MDND 0.1UF 50V Z5U	SR215E104ZAT	AVX	100.4102	60
C8 C72	CAP,FX VALUE,DP MICA 12PF 5% -20+100PPM/C 500V	CM05ED120J03	CDE	101.0120	2
C20 C83	CAP,FX VALUE,DP MICA 22PF 5% -20+100PPM/C 300V	CM05ED220J03	CDE	101.0220	2
C100 C104 C109 C38 C38 C44 C47 C97	CAP FX VAL,DP MICA 36PF 5% -20+100PPM/C 300V	CM05ED360J03	CDE	101.0360	8
C29 C91	CAP FX VAL,DP MICA 68PF 5% -20+100PPM/C 300V	CM05ED680J03	CDE	101.0680	2
C5 C69	CAP FX VAL,DP MICA 100PF 5% 0 TO +70PPM/C 500V	CM05FD101J03	CDE	101.1100	2

WAVETEK PARTS LIST	TITLE: PCA, MAINBOARD 553	ASSEMBLY NO. 1100-00-2872	REV C

PAGE 1

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO	QTY/PT
C1 C13 C65 C77	C: FX PLSTR .47UF 5% 100V	A118474J	BIMO	108.4470	4
C2 C4 C66 C68	C: VAR CER 3.5-18PF 250V	9373	JACO	108.0180	4
C102 C111 C114 C117 C31 C40 C49 C52 C55 C93	C: VAR CER 15-60PF	538-011-F	MILQY	108.0600	10
C19 C21 C22 C23 C24 C84 C85 C86	C: FX TANT .10UF 20% 35V	T368A104M035AS	KEMET	109.4100	8
C123 C124 C127 C130 C131 C132 C133 C134 C135 C136 C137 C138 C139 C140 C141 C142 C143 C144 C145 C146 C147 C148 C149 C150 C151 C152 C153 C25 C87	C: FX TANT 10UF 20% 20V	T368B106M025AS	KEMET	109.6100	29
C160	C: FX ELECT 10UF 25V	3073BA100TG25JPA	MEPCO	109.6102	1
C159 C161	C: FX ELECT 47UF 20% 63V	841283	BIECO	109.6470	2
R104 R133 R144 R19 R218 R30	R: FX MFLM 590 OHM 1% 1/8W TO	RN55C5900F	JNAR	110.5900	6
R131 R17	R: FX MFLM 750 OHM 1% 1/10W T2	RN59C7500F	UNCEN	110.7501	2
R123 R13 R146 R150 R39 R40	R: FX MFLM 1.00K 1% 1/10W T2	RN59C1001F	UNCEN	111.1001	6

WAVETEK PARTS LIST	TITLE: PCA, MAINBOARD 553	ASSEMBLY NO. 1100-00-2872	REV C

PAGE 3

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO	QTY/PT
R113 R3	R: FX MFLM 10.0K 1% 1/10W T2	RN59C1002F	UNCEN	112.1001	2
R204 R76	R: FX MFLM 19.90K .1% 1/8W TO	HA55 100PPM	HYMEG	112.1599	2
R12 R124	R: FX MFLM 16.9K 1% 1/8W TO	RN55C1692F	UNCEN	112.1690	2
R137 R48	R: FX MFLM 17.8K 1% 1/8W TO	RN59C1782F	UNCEN	112.1780	2
R100 R213	R: FX MFLM 19.38K .1% 1/8W TO	HA55 100PPM	HYMEG	112.1939	2
R195 R197 R198 R203 R207 R208 R209 R51 R53 R54 R77 R79 R80 R81	R: FX MFLM 20.5K 1% 1/8W TO	RN55C2052F	UNCEN	112.2050	14
R138 R49	R: FX MFLM 35.7K 1% 1/8W TO	RN59C3572F	UNCEN	112.3570	2
R139	R: FX MFLM 44.2K 1% 1/8W TO	RN59C4422F	UNCEN	112.4420	1
R203 R74	R: FX MFLM 46.75K .5% 1/8W TO	CR125 100PPM	CTLRE	112.4678	2
R199 R55	R: FX MFLM 60.4K 1% 1/10W T2	RN59C6042F	UNCEN	112.6041	2
R160	R: FX MFLM 88.7K 1% 1/8W TO	RN59C8872F	UNCEN	112.8870	1

WAVETEK PARTS LIST	TITLE: PCA, MAINBOARD 553	ASSEMBLY NO 1100-00-2872	REV C

PAGE 5

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO	QTY/PT
C26 C88	CAP FX VAL,DP MICA 200PF 5% 0 TO +70PPM/C 500V	CM05FD201J03	CDE	101.1200	2
C3 C67	CAP,FX VAL,DP MICA 390PF 5% 0 TO+70PPM/C 300V	CM03FD391J03	CDE	101.1390	2
C176	CAP,FX VAL,DIP MICA 300PF 5% 0 TO+70PPM/C 500V	CD15FD301J03	CDE	101.1300	1
C30 C92	CAP,FX VAL,DIP MICA 820PF 1% 0 TO+70PPM/C 300V	CD15FC821F03	CDE	101.1821	2
C101 C105 C110 C34 C39 C43 C48 C96	CAP,FX VAL,DIP MICA 910PF 1% 0 TO+70PPM/C 100V	CD15FA911F03	CDE	101.1910	8
C104 C108 C28 C33 C37 C42 C46 C90 C93 C99	C: FX PLYSTY .01UF -.5+0%	PEBPC0103E	AMRAD	104.3106	10
C27 C89	C: FX PLYCRB 0.1UF -.5+0% 100V	MPABPC0104E	AMRAD	104.4103	2
C103 C107 C32 C36 C41 C45 C94 C98	C: FX PLYSTY 0.1UF 50V SET	PSMO104F-MS	AMRAD	104.4107	4
C162	C: FX PLSTR .10UF 10% 600V	DMT6P1	C-D	105.4100	1

WAVETEK PARTS LIST	TITLE: PCA, MAINBOARD 553	ASSEMBLY NO. 1100-00-2872	REV C

PAGE 2

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO	QTY/PT
R109 R130 R16 R221	R: FX MFLM 1.62K 1% 1/8W TO	RN59C1621F	UNCEN	111.1620	4
R44	R: FX MFLM 1.74K 1% 1/10W T2	RN59C1741F	UNCEN	111.1741	1
R103 R217	R: FX MFLM 2.00K 1% 1/10W T2	RN59C2001F	UNCEN	111.2001	2
R118 R6	R: FX MFLM 2.40K 5% 2W 200PPM	FP42 2.4K 5% 2W 200PPM	CORNG	111.2403	2
R134 R23 R262 R264	R: FX MFLM 3.92K 1% 1/10W T2	NA	NA	111.3921	4
R104 R216	R: FX MFLM 4.32K 1% 1/10W T2	RN59C4321F	UNCEN	111.4321	2
R153	R: FX MFLM 4.42K 1% 1/10W T2	RN59C4421F	UNCEN	111.4421	1
R135 R24	R: FX MFLM 4.99K 1% 1/10W T2	RN59C4991F	UNCEN	111.4991	2
R202 R75	R: FX MFLM 7.027K .1% 1/8W TO	HA55 100PPM	HYMEG	111.7028	2
R46	R: FX MFLM 7.15K 1% 1/8W TO	NA	NA	111.7150	1
R154 R47	R: FX MFLM 8.87K 1% 1/8W TO	RN59C8871F	NA	111.8870	2

WAVETEK PARTS LIST	TITLE: PCA, MAINBOARD 553	ASSEMBLY NO. 1100-00-2872	REV C

PAGE 4

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO	QTY/PT
R112 R3	R: FX MFLM 100K 1% 1/10W T2	RN59C1003F	UNCEN	113.1001	2
R161	R: FX MFLM 178K 1% 1/8W TO	RN59C1783F	UNCEN	113.1780	1
R162	R: FX MFLM 357K 1% 1/8W TO	RN59C3573F	CTLRE	113.3570	1
R116 R4	R: FX MFLM 900K 1% 1/10W T2			113.9009	2
R148 R152 R35 R42	R: FX CFLM 10 OHM 5% 1/4W			116.0101	4
R110 R222	R: FX CFLM 51 OHM 5% 1/4W			116.0511	2
R113	R: FX CFLM 82 OHM 5% 1/4W			116.0821	1
R236 R237 R238 R239 R240 R241 R242 R243 R244 R245 R246 R247 R248 R249 R250 R251 R252 R253 R254 R255 R256 R257 R258 R259 R277	R: FX CFLM 100 OHM 5% 1/4W			116.1101	25
R230 R231 R232	R: FX CFLM 150 OHM 5% 1/4W			116.1151	3
R268	R: FX CFLM 680 OHM 5% 1/4W			116.1681	1

WAVETEK PARTS LIST	TITLE: PCA, MAINBOARD 553	ASSEMBLY NO. 1100-00-2872	REV C

PAGE A

NOTE UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN	DATE	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL	PROJENGR		TITLE: PARTS LIST MAIN BOARD ASSEMBLY
	RELEASE APPROV		
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ± .010 ANGLES ± 1 XX ± .030		
	DO NOT SCALE DWG	MODEL NO 553A	DWG NO 1100-00-2872 REV C
	SCALE	TOOL IDENT 23338	SHEET 1 OF 4

THIS DOCUMENT CONTAINS PROPRIETARY INFORMATION AND DESIGN RIGHTS BELONGING TO WAVETEK AND MAY NOT BE REPRODUCED FOR ANY REASON EXCEPT CALIBRATION, OPERATION, AND MAINTENANCE WITHOUT WRITTEN AUTHORIZATION

REV	ECN	BY	DATE	APP

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO	QTY/PT
R224 R233 R234 R235 R266	R: FX CFLM 1.0K OHM 5% 1/8W			116.2100	5
R226 R228	R: FX CFLM 1.5K OHM 5% 1/4W			116.2151	2
R227 R229	R: FX CFLM 3.0K OHM 5% 1/4W			116.2301	2
R119 R120 R147 R34 R7 R8	R: FX CFLM 4.7K OHM 5% 1/4W			116.2471	6
R270 R271	R: FX CFLM 5.6K OHM 5% 1/4W			116.2561	2
R111 R153 R201 R211 R223 R225 R260 R261 R275 R36 R37 R83	R: FX CFLM 10K OHM 5% 1/4W			116.3101	12
R127 R128 R129 R136 R141 R142 R20 R21 R22 R25 R26 R31 R32	R: FX CFLM 47K OHM 5% 1/4W			116.3471	13
R267 R269	R: FX CFLM 68K OHM 5% 1/4W			116.3681	2
R139 R154 R272 R38	R: FX CFLM 100K OHM 5% 1/4W			116.4101	4
R107 R219 R26	R: FX CFLM 470K OHM 5% 1/4W			116.4471	3

WAVETEK PARTS LIST | TITLE: PCA. MAINBOARD 553 | ASSEMBLY NO. 1100-00-2872 | REV C

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO	QTY/PT
U10 U34	U: QUAD ANAL VOLT COMP (LM339)	LM339N	MOT	120 3339	2
U20 U39	U: HEX MOS-LED DRIVER (75494)	75494N	NSC	120 4494	2
U70 U71 U87 U88 U89	U: OPTO-ISOLATOR (TIL-112)	TIL-112	TI	120.9112	5
S3	CONN CABLE & POB PLUG (MOLEX)	03-09-2062	MOLEX	351.0601	1
S3	SOCKET: CRIMP FEM .093 (MOLEX)	02-09-1103	MOLEX	353.0109	1
S3	TIE CABLE NY NAT 3/4 MAX DIA	SST-1-M	PANDT	377 4001	1
S3	WIRE, #22 AWG STR BLACK			378.1604	1
S3	WIRE, #22 AWG STR WHITE			378.1694	1
S3	SHRINK TBG PLYFIN BLACK 3/16"			378.5330	1
S3	SWITCH ASSY PB	5103-00-0020	WVTK	5102-00-0005	1
U1 U25	U: HEX INVERT DRIVER O/C			122 7406	2
U58 U62	U: 3 TO 8 LINE DECOD	74LS138N/AT	NSC	125 0113	2

WAVETEK PARTS LIST | TITLE: PCA. MAINBOARD 553 | ASSEMBLY NO. 1100-00-2872 | REV C

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO	QTY/PT
U83 U84 U85	U: PULL UP NET 10K 2% X9 SIP	110A103	AB	128 3104	3
U57	U: SRAM 2048 X 8 NMOS	TMS4016-15N	TI	129 3032	1
U53	MICRO PROCESSOR (2 MHZ, Z80)	MK3880N	MOSTK	129 3201	1
U63	MC6848B-MH	MC6848P	MOT	129 3202	1
CR116 CR117 CR118	SIL RCT 600PIV 1A (1N4937)			130 4110	3
CR1 CR106 CR108 CR2 CR53 CR55 CR56 CR57	SL ZR 5.1V 5% 400MW (1N751A)			131 9510	8
CR10 CR100 CR101 CR102 CR103 CR104 CR103 CR107 CR109 CR11 CR110 CR111 CR112 CR113 CR114 CR115 CR119 CR12 CR120 CR121 CR122 CR13 CR14 CR15 CR16 CR17 CR18 CR19 CR20 CR21 CR22 CR23 CR24 CR25 CR26 CR27 CR28 CR29 CR3 CR30 CR31 CR32 CR33 CR34 CR35 CR36 CR37 CR38 CR39 CR4 CR40 CR41 CR42 CR43 CR44 CR45 CR46 CR47 CR48 CR49 CR5 CR50 CR51 CR52 CR54 CR58 CR59 CR6 CR60 CR61 CR62 CR63 CR64 CR65 CR66	SL LW LK 70P1V 200MW (1N457)			132 0457	111

WAVETEK PARTS LIST | TITLE: PCA. MAINBOARD 553 | ASSEMBLY NO 1100-00-2872 | REV C

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO	QTY/PT
R117 R138 R14 R151 R27 R41	R: FX CFLM 1.0M OHM 5% 1/4W			116.3101	6
R103 R11 R123 R215	R: VAR CMT 300 OHM 3/8SQ FM	72PR300	BECK	118.1303	4
R210 R82	R: VAR CMT 1.0K 3/8SQ FM	72PR1K	BECK	118.2102	2
R200 R56	R: VAR CMT 3.0K 3/8SQ FM	72PR3K	BECK	118.2302	2
R126 R140 R15 R28	R: VAR CMT 10K 3/8SQ FM	72PR10K	BECK	118.3101	4
R108 R220	R: VAR CMT 100K 3/8SQ FM			118.4103	2
U12 U19 U28 U29 U33 U38 U4 U5 U94 U95	U: LIN BIFET OP-AMP DIL LF351	LF351N	NSC	120 1017	10
U27 U3	U LIN OP-AMP DIL (NE5534A)	SA5534AN	SIG	120.1018	2
U13 U14 U36 U37	U: GD LIN BIFET OP-AMP (LF347)	LF347N	NSC	120.2047	4
U21 U22 U30 U31 U43 U44 U6 U7	U: GD LIN OP-AMP (LM324N)	LM324N	NSC	120.2324	8
U64 U65	U: IEEE 8U8 XCVR (MC3447P)	MC3447P	MOT	120.2447	2

WAVETEK PARTS LIST | TITLE: PCA. MAINBOARD 553 | ASSEMBLY NO. 1100-00-2872 | REV C

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO	QTY/PT
	(74LS138)				
U23 U32 U42 U8	U: OCT D-FLIP W/CLR (74LS273)			125 0139	4
U69 U82	U: OCT BUF INV 3-ST (74LS240)	74LS240N/P3	TI	125.0144	2
U34 U35 U59	U: OCT BUF 3-ST (74LS244)	74LS244N/S28	SIG	125 0153	3
U56	U: OCT BUS XCVR 3ST (74LS245)	74LS245N/P3	TI	125.0154	1
U80 U90	U: QUAD 2 IN NAND GATE	74LS00N/S28	TI	125 7400	2
U81	U: QUAD 2IN NOR GATE	74LS02N/S	TI	125 7402	1
U73 U74 U76	U: HEX INVERTER	74LS04N/S28	SIG	125 7404	3
U93	U: HEX SMT TRGR	74LS14N/DS	MOT	125.7414	1
U75	U: DUAL 4 IN NAND GATE	74LS20NDS	RAYTH	125.7420	1
U77 U78 U79	U: QUAD 2 IN OR GATE	74LS32N/S28	SIG	125 7432	3
U61	U: DUAL TYPE D FLIP FLOP	74LS74N/P3	SIG	125.7474	1
U28 U40	U: PULL UP NET 1K 2% X7 SIP	4308R-101-102	BOURN	128 2103	2

WAVETEK PARTS LIST | TITLE: PCA. MAINBOARD 553 | ASSEMBLY NO. 1100-00-2872 | REV C

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO	QTY/PT
CR67 CR68 CR69 CR7 CR70 CR71 CR72 CR73 CR74 CR75 CR76 CR77 CR78 CR79 CR8 CR80 CR81 CR82 CR83 CR84 CR85 CR86 CR87 CR88 CR89 CR9 CR90 CR91 CR92 CR93 CR94 CR95 CR96 CR97 CR98 CR99					
Q102	Q: SIL NPN (2N2222)	2N2222A	MOT	134 2222	1
Q101	Q: SIL PNP (2N4122)			136 4122	1
Q30 Q60	Q SIL PNP (2N4249)			136 4249	2
U2 U26	Q DL MATCH FET (NPD-5566)	NPD-5566	NSC	138 5566	2
Q10 Q100 Q11 Q12 Q13 Q14 Q15 Q16 Q17 Q18 Q19 Q20 Q21 Q22 Q23 Q24 Q25 Q26 Q27 Q28 Q29 Q3 Q30 Q31 Q32 Q33 Q34 Q35 Q36 Q37 Q38 Q39 Q4 Q40 Q41 Q42 Q43 Q44 Q45 Q46 Q47 Q48 Q49 Q5 Q53 Q54 Q55 Q56 Q57 Q58 Q59 Q6 Q61 Q62 Q63 Q64 Q65 Q66 Q67 Q68 Q69 Q70 Q71 Q72 Q73 Q74 Q75 Q76 Q77 Q78 Q79 Q8 Q80 Q81 Q82 Q83 Q84 Q85 Q86 Q87 Q88 Q89 Q9 Q90 Q91 Q92 Q93 Q94 Q95 Q96 Q97 Q98 Q99	Q: FET N-CHAN JCT	2N5638-5	NSC	138 5638	93

WAVETEK PARTS LIST | TITLE: PCA. MAINBOARD 553 | ASSEMBLY NO. 1100-00-2872 | REV C

NOTE UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES | MATERIAL | FINISH WAVETEK PROCESS | DRAWN | DATE | PROJ/ENGR | RELEASE APPROV | TOLERANCE UNLESS OTHERWISE SPECIFIED XX = .010 ANGLES = 1 XX = .030 | DO NOT SCALE DWG | SCALE

WAVETEK SAN DIEGO, CALIFORNIA

TITLE: PARTS LIST MAIN BOARD ASSEMBLY

MODEL NO 553A | DWG NO 1100-00-2872 | REV C | CAGE CODE 23338 | SHEET 2 OF 4

BISHOP GRAPHICS/ACCUPRESS REORDER NO. A1884

THIS DOCUMENT CONTAINS PROPRIETARY INFORMATION AND DESIGN RIGHTS BELONGING TO WAVETEK AND MAY NOT BE REPRODUCED FOR ANY REASON EXCEPT CALIBRATION, OPERATION, AND MAINTENANCE WITHOUT WRITTEN AUTHORIZATION

REV	ECN	BY	DATE	APP

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO	QTY/PT
NONE	SPRING REF. 3200-01-0001	147-383	WVTK	1400-00-3730	1
NONE	BRKT, POWER ROD	182-310	WVTK	1400-00-5163	2
NONE	PUSHROD, POWER	352-0210	WVTK	1400-02-0210	1
NONE	STIFFNER, PCB	ST-16.16	CONFB	1400-02-0490	1
NONE	WASHER	352-0983	WVTK	1400-02-0983	4
L1 L2 L3	L: FXD 1 PHY MI-CURR	6310-12	CADBU	150.2101	3
NONE	DRILL DRWG MAIN BD	1700-00-2364	WVTK	1700-00-2364	1
K14 K15 K19 K20 K21 K28 K5 K6 K7	RELAY REED DIP 1A W/DIODE 5V	1503-8-1	WABSH	175.1503	9
K10 K11 K12 K13 K16 K17 K18 K2 K22 K23 K24 K25 K26 K27 K3 K4 K8 K9	RELAY REED DIP 2A W/DIODE 5V	1503-7-1	WABSH	175.1507	18
J2	CONNECTOR, 9PIB, RT ANGLE PC MOUNT	68519-001	BERG	2100-02-0198	1
J3	CONNECTOR, D-SUB, MDR, P C MOUNT	67711-025	BERG	2100-02-0199	1
J4	CONNECTOR, HEADER, 8 PIN, 0 156 SPACE	09-65-1081	MOLEX	2100-02-0219	1
S1 S2	S: DIP 8 POLE 2 POS	76B08	GRAHL	342 8100	2

WAVETEK PARTS LIST | TITLE: PCA, MAINBOARD 553 | ASSEMBLY NO. 1100-00-2872 | REV C

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO	QTY/PT
NONE	M SCR SS PHP 2-56 X 1/4 PH			385 2042	2
NONE	M SCR: SS PHP 4-40 X 3/8 PH			385.4062	11
NONE	NUT: HEX SS 2-56 X 5/32AB			387.2051	2
NONE	NUT: HX ST CD 4-40 X 3/16AF			387.4060	8
NONE	WASHER: INT LK STL CAD #2			388.1020	2
NONE	WASHER: SPLT LK STNLS #4			388.1042	8
NONE	WASHER FLT NYL #4 1/4D X 1/8T			388.3040	3
NONE	SPR, NYL 1/4" RND #6 X 312			389.2029	3
R274	VAR CMT 200K 15T	3006-1-204	BOURN	4600-12-0403	1
R101 R102 R212 R214	RES, MF, 1/8W, 1%, 600	RN55D-6000B	TRW	4701-02-6000	4
R10 R121 R122 R9	RES, MF, 1/8W, 1%, 2.87K	RN55D-2871F	TRW	4701-03-2871	4
R263 R265	RES, MF, 1/8W, 1%, 3.24K	RN55D-3241F	TRW	4701-03-3241	2
R196 R52	RES, MF, 1/8W, 1%, 3.23K	RN55D-3231F	MEPCO	4701-03-3231	2

WAVETEK PARTS LIST | TITLE: PCA, MAINBOARD 553 | ASSEMBLY NO. 1100-00-2872 | REV C

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO	QTY/PT
	K				
R179 R187	RES, MF, 1/8W, , 1%, 2.637 K	MM55-2.637K-, 1-100	HYMEG	4799-00-0116	2
R163 R173	RES, MF, 1/8W, , 1%, 7.630 K	MM55-7.630K-, 1-100	HYMEG	4799-00-0117	2
R166 R174	RES, MF, 1/8W, , 1%, 18.30 K	MM55-18.30K-, 1-100	HYMEG	4799-00-0118	2
R167 R175	RES, MF, 1/8W, , 1%, 19.12 K	MM55-19.12K-, 1-100	HYMEG	4799-00-0119	2
R168 R176	RES, MF, 1/8W, , 1%, 30.30 K	MM55-30.30K-, 1-100	HYMEG	4799-00-0120	2
R163 R171	RES, MF, 1/8W, , 1%, 1 885 K	MM55-1 885K- 1-100	HYMEG	4799-00-0121	2
R164 R172	RES, MF, 1/8W, , 1%, 3.800 K	MM55-3.800K-, 1-100	HYMEG	4799-00-0122	2
R84 R92	RES, MFLM, 1.455K, , 1%, 1 /8W, TO	MM-55-1.455K-, 1-100PPM	HYMEG	4799-00-0124	2
R83 R93	RES, MFLM, 2.940K, , 1%, 1 /8W, TO	MM-55-2.940K-, 1-100PPM	HYMEG	4799-00-0125	2
R86 R94	RES, MFLM, 5 910K, , 1%, 1 /8W, TO	MM-55-5 910K-, 1-100PPM	HYMEG	4799-00-0126	2
R87 R95	RES, MFLM, 11.83K, , 1%, 1	MM-55-11.83K-, 1-100PPM	HYMEG	4799-00-0127	2

WAVETEK PARTS LIST | TITLE: PCA, MAINBOARD 553 | ASSEMBLY NO. 1100-00-2872 | REV C

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO	QTY/PT
J5 J6 J7 J8	CONN COAX BLKHD RECPT 180L	31-010	AMPH	351.0006	4
E1 E13 E14 E6 E7 E8	PLUG SHORTING (LOW PROF)	4612872-01-03-10	CTC	352.0202	6
NONE	SOCKET: JMPR (USE W/352 0202)	4503327-01-0300	CTC	353.0104	12
XU13 XU14 XU36 XU37	SOCKET: IC 14PIN DIP ST			353.1403	4
XS1 XS2	SOCKET: IC 16PIN DIP 1ST	16-823-90	ARIES	353.1605	2
XU60	SOCKET: IC 28PIN DIP ST			353.2800	1
XU53	SOCKET: IC 40PIN DIP ST			353.4001	1
J1	CONN: TERM 34 PIN DIL	929665-01-17	A/P	354.0005	1
TP1 TP10 TP11 TP12 TP2 TP3 TP4 TP5 TP6 TP7 TP8 TP9	CONN TERM PIN .025 MM (.2END)	M239-025-5006	A/S	354.0007	12
NONE	1" WIDE BROWN URETHANE TAPE	SJ 3832	3M	377.0201	2
NONE	WIRE, #22 AWG BON BLACK			378.1609	3

WAVETEK PARTS LIST | TITLE: PCA, MAINBOARD 553 | ASSEMBLY NO. 1100-00-2872 | REV C

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO	QTY/PT
R145 R149 R206 R33 R37 R78	RES, MF, 1/8W, 1%, 9.09K	RN55D-9091F	TRW	4701-03-9091	6
R114 R2	RES, MF, 1/4W, 1%, 1M	RN60D-1004F	TRW	4701-13-1004	2
U11 U15 U16 U17 U18 U45 U46 U48 U49 U50	PULL UP NET 47K 2% X9 SIP	750-101-R47K	CTS	4770-00-0047	10
R169 R177	RES, MF, 1/8W, , 1%, 76.80 K	MM55-76.80K-, 1-100	HYMEG	4799-00-0107	2
R170 R178	RES, MF, 1/8W, , 1%, 153.20 OK	MM55-153.20K-, 1-100	HYMEG	4799-00-0108	2
R132 R143 R18 R180 R198 R29	RES, MF, 1/8W, , 1%, 3.304 K	MM55-3.304K-, 1-100	HYMEG	4799-00-0109	6
R181 R189	RES, MF, 1/8W, , 1%, 10.64 K	MM55-10.64K-, 1-100	HYMEG	4799-00-0110	2
R182 R190	RES, MF, 1/8W, , 1%, 21.31 K	MM55-21.31K-, 1-100	HYMEG	4799-00-0111	2
R183 R191	RES, MF, 1/8W, , 1%, 26.64 K	MM55-26.64K-, 1-100	HYMEG	4799-00-0112	2
R184 R192	RES, MF, 1/8W, , 1%, 53.32 K	MM55-53.32K-, 1-100	HYMEG	4799-00-0113	2
R185 R193	RES, MF, 1/8W, , 1%, 106.7 K	MM55-106.7K-, 1-100	HYMEG	4799-00-0114	2
R186 R194	RES, MF, 1/8W, , 1%, 213.4	MM55-213.4K-, 1-100	HYMEG	4799-00-0115	2

WAVETEK PARTS LIST | TITLE: PCA, MAINBOARD 553 | ASSEMBLY NO. 1100-00-2872 | REV C

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO	QTY/PT
	/8W, TO				
R98 R96	RES, MFLM, 14.82K, , 1%, 1 /8W, TO	MM-55-14.82K-, 1-100PPM	HYMEG	4799-00-0128	2
R89 R97	RES, MFLM, 29.70K, , 1%, 1 /8W,	MM55-29.70K-, 1-100PPM	HYMEG	4799-00-0129	2
R90 R98	RES, MFLM, 39.40K, , 1%, 1 /8W, TO	MM55-39.40K-, 1-100PPM	HYMEG	4799-00-0130	2
R91 R99	RES, MFLM, 118.8K, , 1%, 1 /8W, TO	MM55-118.8K-, 1-100PPM	HYMEG	4799-00-0131	2
R58 R66	RES, MFLM, 2.038K, , 1%, 1 /8W, TO	MM55-2.038K-, 1-100PPM	HYMEG	4799-00-0132	2
R59 R67	RES, MFLM, 4.107K, , 1%, 1 /8W, TO	MM55-4.107K-, 1-100PPM	HYMEG	4799-00-0133	2
R60 R68	RES, MFLM, 8.243K, , 1%, 1 /8W, TO	MM55-8.243K-, 1-100PPM	HYMEG	4799-00-0134	2
R61 R69	RES, MFLM, 16.52K, , 1%, 1 /8W, TO	MM55-16.52K-, 1-100PPM	HYMEG	4799-00-0135	2
R62 R70	RES, MFLM, 20.65K, , 1%, 1 /8W, TO	MM55-20.65K-, 1-100PPM	HYMEG	4799-00-0136	2
R63 R71	RES, MFLM, 41.34K, , 1%, 1 /8W, TO	MM55-41.34K-, 1-100PPM	HYMEG	4799-00-0137	2
R64 R72	RES, MFLM, 82.72K, , 1%, 1	MM55-82.72K-, -, 1-100PPM	HYMEG	4799-00-0138	2

WAVETEK PARTS LIST | TITLE: PCA, MAINBOARD 553 | ASSEMBLY NO. 1100-00-2872 | REV C

NOTE UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES | MATERIAL | FINISH WAVETEK PROCESS | DRAWN | DATE | PROJENGR | RELEASE APPROV | TOLERANCE UNLESS OTHERWISE SPECIFIED XXX - .010 ANGLES - 1 XX - .030 | DO NOT SCALE DWG | SCALE

WAVETEK SAN DIEGO • CALIFORNIA

TITLE: PARTS LIST MAIN BOARD ASSEMBLY

MODEL NO 553A | DWG NO 1100-00-2872 | REV C | CODE IDENT 23338 | SHEET 3 OF 4

BISHOP GRAPHICS/ACCUPRESS REORDER NO A-3884

THIS DOCUMENT CONTAINS PROPRIETARY INFORMATION AND DESIGN RIGHTS BELONGING TO WAVETEK AND MAY NOT BE REPRODUCED FOR ANY REASON EXCEPT CALIBRATION, OPERATION, AND MAINTENANCE WITHOUT WRITTEN AUTHORIZATION

REV	ECN	BY	DATE	APP

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
	/8W, TO				
R65 R73	RES. MFLM. 165 5K, 1%, 1 /8W, TO	MN55-165 5K- 1-100PPM	HYMEQ	4799-00-0139	2
R43	RES. MFLM. 866. 1%. 1/8W. TO	[illegible]	TRW	4799-00-0140	1
R45	RES. MFLM. 3 48K, 1%, 1/8 W, TO	RN55D3481F	TRW	4799-00-0141	1
R50	RES. MFLM. 71. 5K, 1%, 1/8 W, TO	RN55D7152F	TRW	4799-00-0142	1
Q103	TRANS. NPN. PLANAR POWER	D44C11	NSC	4902-04-4110	1
U51	OSC 10.24MHZ	K1100-A	MOT	[illegible]	1
U66	[illegible] DRIVER. RS-232C	MC1488	MOT	8000-14-0800	1
U67	[illegible] RECEIVER. RS-232C	MC1489L	MOT	[illegible]	1
U68	ASYN COMM ELEM (INS8250)	[illegible]	NSC	8000-82-3000	1
U91 U92	SHFT REG 8B SIPO. TTL	74LS164	TI	8007-41-6410	2
U24 U33 U41 U86 U9	D-F/F. QUAD. TTL	74LS175	TI	8007-41-7510	3
U52	CNTR. DUAL 4B DCD. TTL	74LS390	TI	8007-43-9010	1

WAVETEK PARTS LIST	TITLE: PCA. MAINBOARD 553	ASSEMBLY NO: 1100-00-2872	REV: C

[illegible]

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
U60	IC, PROGRAMMED 552 REF 8002-71-2800	8600-00-0370	WVTK	8600-00-0370	1

WAVETEK PARTS LIST	TITLE: PCA. MAINBOARD 553	ASSEMBLY NO: 1100-00-2872	REV: C

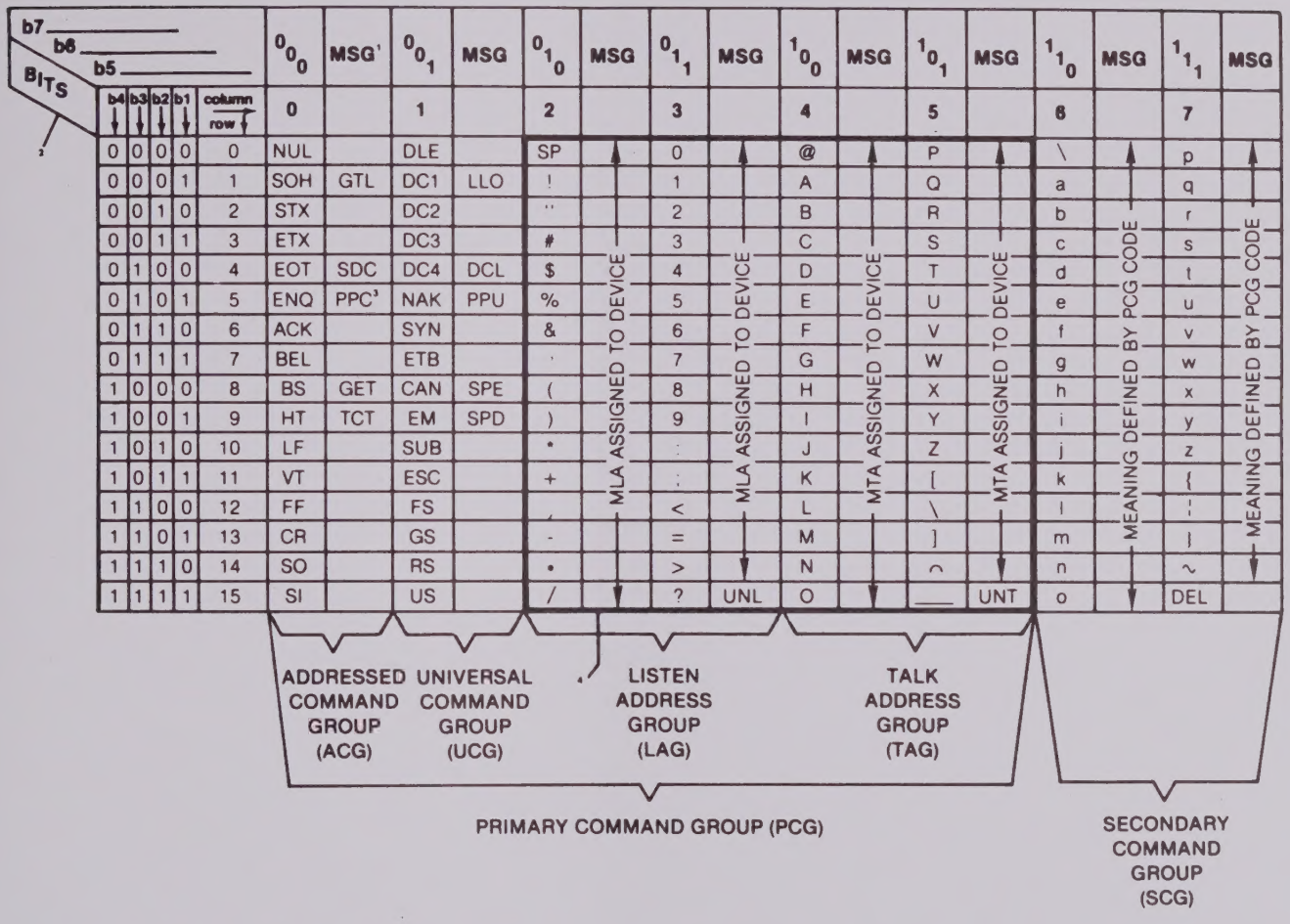
NOTE UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN	DATE	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL	PROJ ENGR		TITLE: PARTS LIST MAIN BOARD ASSEMBLY
FIN SH WAVETEK PROCESS	RELEASE APPROV		
	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ± .010 ANGLES ± 1 XX ± .030		
	DO NOT SCALE DWG		MODEL NO: 553A / DWG NO: 1100-00-2872 / REV: C
	SCALE		CODE IDENT: 23338 / SHEET: 4 OF 4

BISHOP GRAPHICS/ACCUPRESS RECORDER NO. A-5994

APPENDIX A

American Standard Code for Information Interchange (ASCII)



b4	b3	b2	b1	column / row	0	MSG[1]	1	MSG	2	MSG	3	MSG	4	MSG	5	MSG	6	MSG	7	MSG
0	0	0	0	0	NUL		DLE		SP		0		@		P		\		p	
0	0	0	1	1	SOH	GTL	DC1	LLO	!		1		A		Q		a		q	
0	0	1	0	2	STX		DC2		"		2		B		R		b		r	
0	0	1	1	3	ETX		DC3		#		3		C		S		c		s	
0	1	0	0	4	EOT	SDC	DC4	DCL	$		4		D		T		d		t	
0	1	0	1	5	ENQ	PPC[3]	NAK	PPU	%		5		E		U		e		u	
0	1	1	0	6	ACK		SYN		&		6		F		V		f		v	
0	1	1	1	7	BEL		ETB		'		7		G		W		g		w	
1	0	0	0	8	BS	GET	CAN	SPE	(		8		H		X		h		x	
1	0	0	1	9	HT	TCT	EM	SPD	)		9		I		Y		i		y	
1	0	1	0	10	LF		SUB		*		:		J		Z		j		z	
1	0	1	1	11	VT		ESC		+		;		K		[		k		{	
1	1	0	0	12	FF		FS		,		<		L		\		l		|	
1	1	0	1	13	CR		GS		-		=		M		]		m		}	
1	1	1	0	14	SO		RS		.		>		N		^		n		~	
1	1	1	1	15	SI		US		/		?	UNL	O		_	UNT	o		DEL	

[1]MSG = INTERFACE MESSAGE
[2]b1 = DIO1 . . . b7 = DIO7
[3]REQUIRES SECONDARY COMMAND
[4]DENSE SUBSET (COLUMN 2 THROUGH 5)

DC4	= DCL	Device clear	Universal Command Group
DC1	= LLO	Local lockout	
NAK	= PPU	Parallel poll unconfigure	
EM	= SPD	Serial poll disable	
CAN	= SPE	Serial poll enable	
SOH	= GTL	Go to local	Addressed Command Group
EOT	= SDC	Selected device clear	
ENQ	= PPC	Parallel poll configure	
BS	= GET	Group execute trigger	
HT	= TCT	Take control	

MP MASTER
MA35676